Flash 1.8V 2 Gbit SPI-NAND Flash Memory

PRODUCT LIST

Parameters	Values
V_{CC}	1.8V
Width	x1, x2[1], x4
Frequency	83/104 MHz
Internal ECC Correction	8-bit
Transfer Rate	9.6ns
Power-up Ready Time	1.5ms (maximum value)
Max Reset Busy Time	1.5ms (maximum value)

Note: 1. x2 PROGRAM operation is not defined.

FEATURES

- Single Power Supply Voltage: 1.7V~1.95V
- Operation Range: 1.7V~1.95V
- Organization
  - Page size x1: 2176 bytes (2K + 128 bytes)
  - Data Register: (2K + 128) x 8bit
  - Block size: 64 pages
  - Plane size: 2Gb (1 plane, 2048 blocks per plane)
- Automatic Program and Erase
- Page Program Size: (2K + 128) Byte
- Block Erase Size: (128K + 8K) Byte
- User-selectable internal ECC supported
- Internal ECC: 8bits /512Byte
- Deep Power Down Mode
- Boot Read
- Access time
  - Page Read Time (from Cell to Register, with Internal ECC): 130us (Maximum)
- Program/ Erase Speed
  - Program time:400us typical
  - Block Erase time: 4ms typical
- Memory Cell: 1bit/Memory Cell
- Support SPI-Mode 0 and SPI-Mode 3[(1)]
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating Gate Technology
  - Endurance: 60K P/E Cycle Times
  - Uncycled Data Retention: 10 years of real time use at 55°C
- Command Register Operation
- NOP: 4 cycles
- OTP Operation
- Security
  - The first block (Block0) is guaranteed to be a valid block at the time of shipment with ECC enabled
  - Block Protection
  - Program/Erase Lockout During Power Transitions
- Cache Read
- Operating temperature
  - Industrial: -40°C to +105°C

Note: 1. Mode 0: CPOL = 0, CPHA = 0; Mode 3: CPOL = 1, CPHA = 1

ORDERING INFORMATION

Product ID	Speed	Package		Comments
F50D2G41KA-104YIAG2V	104 MHz	8-contact WSON	8x6mm	Pb-free
F50D2G41KA-83YIAG2V	83 MHz			
F50D2G41KA-104YIAG2VE	104 MHz	8-contact WSON (without expose metal pad)	8x6mm	Pb-free
F50D2G41KA-83YIAG2VE	83 MHz			

GENERAL DESCRIPTION

The serial electrical interface follows the industry-standard serial peripheral interface (SPI), providing a cost-effective non-volatile memory storage solution in systems where pin count must be kept to a minimum. The device is a 2Gb SLC SPI-NAND Flash memory device based on the standard parallel NAND Flash, but new command protocols and registers are defined for SPI operation. It is also an alternative to SPI-NOR, offering superior write performance and cost per bit over SPI-NOR.

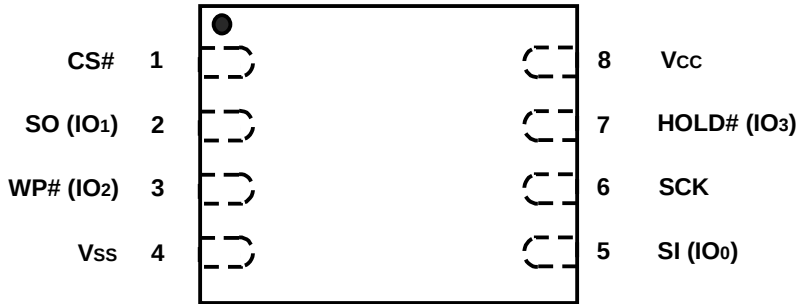
The command-set resembles common SPI-NOR command set, modified to handle NAND-specific functions and new features. New features include user-selectable internal ECC. With internal ECC enabled, ECC code is generated internally when a page is written to the memory array. The ECC code is stored in the spare area of each page. When a page is read to the cache register, the ECC code is calculated again and compared with the stored value. Errors are corrected if necessary. The device either outputs corrected data or returns an ECC error status.

The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased. The device contains 2048 blocks, composed by 64 pages consisting in two NAND structures of 32 series connected Flash cells. Each page consists 2176-Byte and is further divided into a 2048-Byte data storage area with a separate 128-Byte spare area. The 128-Byte area is typically used for memory and error management.

The pins serve as the ports for signals. This Deice has six signal lines plus V_{CC} and ground (GND, V_{SS}). The signal lines are SCK (serial clock), SI (command and data input), SO (response and data output), and control signals CS#, HOLD#, WP#.

PIN CONFIGURATION (TOP VIEW)

8-Contact WSON
(WSON 8C, 8mmx6 mm Body, 1.27mm Contact Pitch)

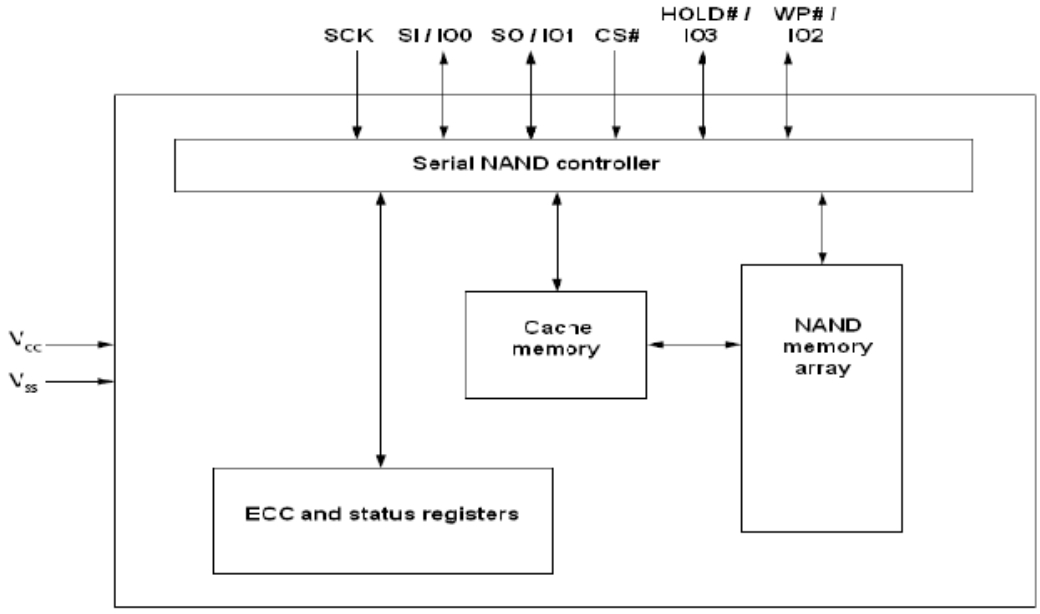


Pin Description

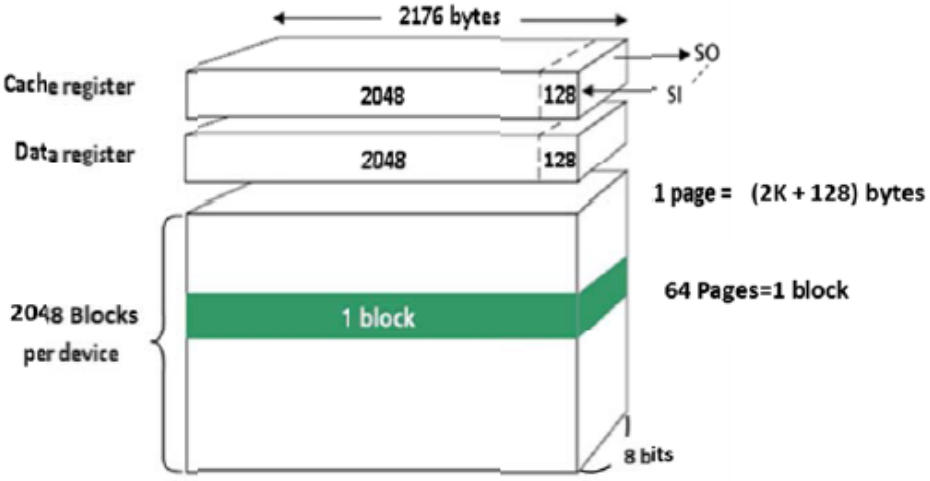
Pin Name	Functions
CS#	**Chip Select (Input)** The device is activated [1]/deactivated [2] as CS# is driven LOW/HIGH. After power-on, the device requires a falling-edge on CS# before any command can be written. The device goes to standby mode when no PROGRAM, ERASE, or WRITE STATUS REGISTER operation is in progress.
SO / IO1	**Serial Data Output (Output) / IO_1 (Input/Output)** SO transfers data serially out of the device on the falling-edge of SCK. SO must not be driven during x2 or x4 PROGRAM operation.
WP# / IO2	**Write Protect (Input) / IO_2 (Input/Output)** WP# is driven LOW to prevent writing the Feature Registers. The WP-E bit in Protection Register controls the function of WP#, and the other bits in Register can protect a specific portion by hardware. When WP-E=1, the device is in the Hardware-protection mode that WP# functions as a dedicated active low input pin for the Write Protect of the device. If WP-E=1 and WP# goes LOW, the device will become READ-only. When WP-E=0, the device is in the Software-protection mode that only Protection Register can be protected. WP# functions as a data I/O pin. WP# must not be driven during x4 operation; it means Write Protect function is only available for standard and x2 SPI.
SI / IO0	**Serial Data Input (Input) / IO_0 (Input/Output)** SI transfers data serially into the device. Device latches addresses, commands, and program data in SI on the rising-edge of SCK. SI must not be driven during x2 or x4 READ operation.
HOLD# / IO3	**Hold (Input) / IO_3 (Input/Output)** Hold pauses any serial communication with the device without deselecting it.[3] When driven LOW, SO is at high impedance (Hi-Z), and all inputs in SI and SCK are ignored; CS# also should be driven LOW.
SCK	**Serial Clock (Input)** SCK provides serial interface timing. Address, commands, and data in SI are latched on the rising edge of SCK. Output (data in SO) is triggered after the falling-edge of SCK. The clock is valid only when the device is active.[4]
V_{CC}[5]	**Power** V_{CC} is the power supply for device.
V_{SS}[5]	**Ground**
NC	**No Connection** Not internally connected.

Note:
1. CS# places the device in active power mode.
2. CS# deselects the device and places SO at high impedance.
3. It means HOLD# input doesn't terminate any READ, PROGRAM, or ERASE operation currently in progress.
4. SI and SO can be triggered only when the clock is valid.
5. Connect all V_{CC} and V_{SS} pins of each device to common power supply outputs. Do not leave V_{CC} or V_{SS} disconnected.

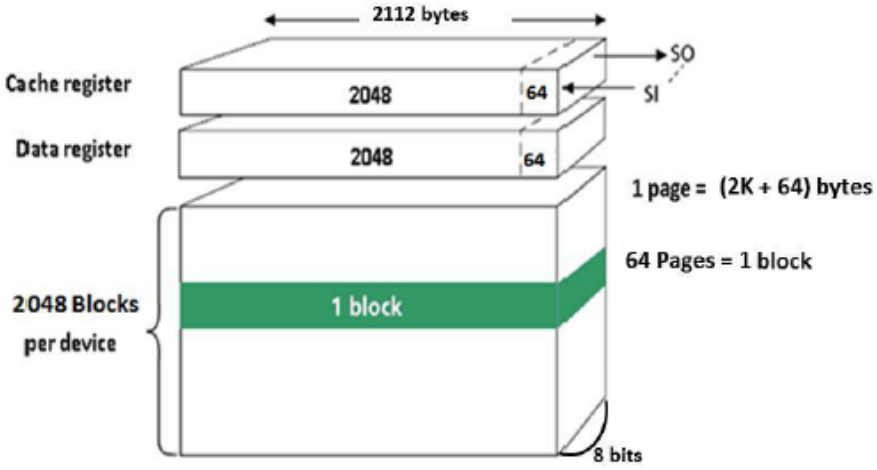
Block Diagram



Functional Block Diagram



Array Organization (Internal ECC=OFF)



Array Organization (Internal ECC=ON)

Addressing

There are two address types used: the column address and the row address. The column address is used to access bytes within a page. The row address is used to address pages and blocks. There are some functions that may require only row addresses, such as Block Erase.

Addressing

- Row Address: 17 bits
  - Block Address (2048 blocks/device): 11 bits, RA [16,6]
  - Page Address (64 pages/block): 6 bits, RA [5,0]
- Column Address (2112 or 2176 bytes/page): 12 bits, CA [11,0]

Device Operation

SPI Mode

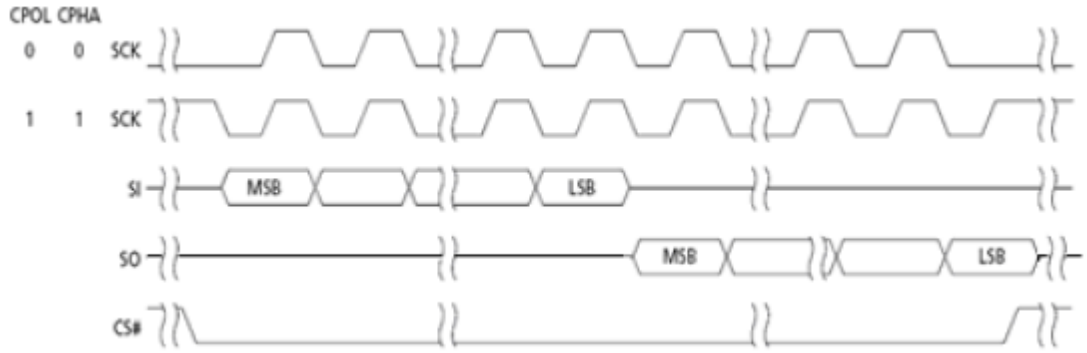
SPI NAND supports two SPI modes:

(Mode 0) CPOL (clock polarity) = 0, CPHA (clock phase) = 0

(Mode 3) CPOL=1, CPHA=1

Input data is latched in on the rising edge of SCK, and output data is available from the falling edge of SCK for both modes. For Mode 0, the CLK signal is normally low on the falling and rising edges of CS#. For Mode 3, the CLK signal is normally high on the falling and rising edges of CS#.

When CS# is high, keep SCK at V_{SS} (Mode 0) or V_{CC} (Mode 3). Do not begin toggling SCK until after CS# is driven LOW.

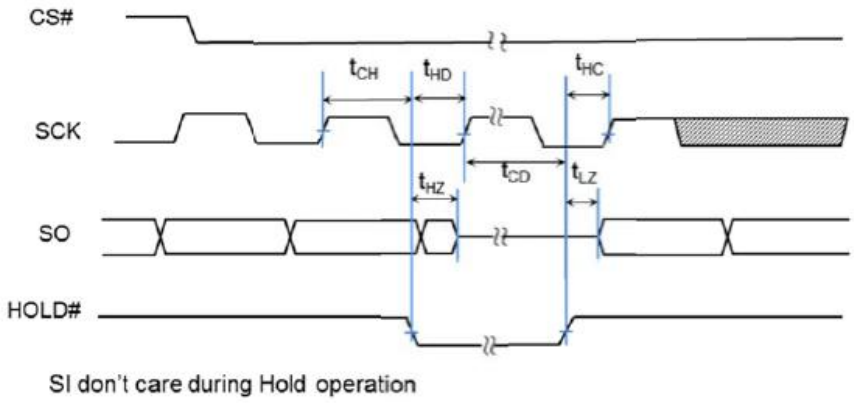


SPI Modes Timing

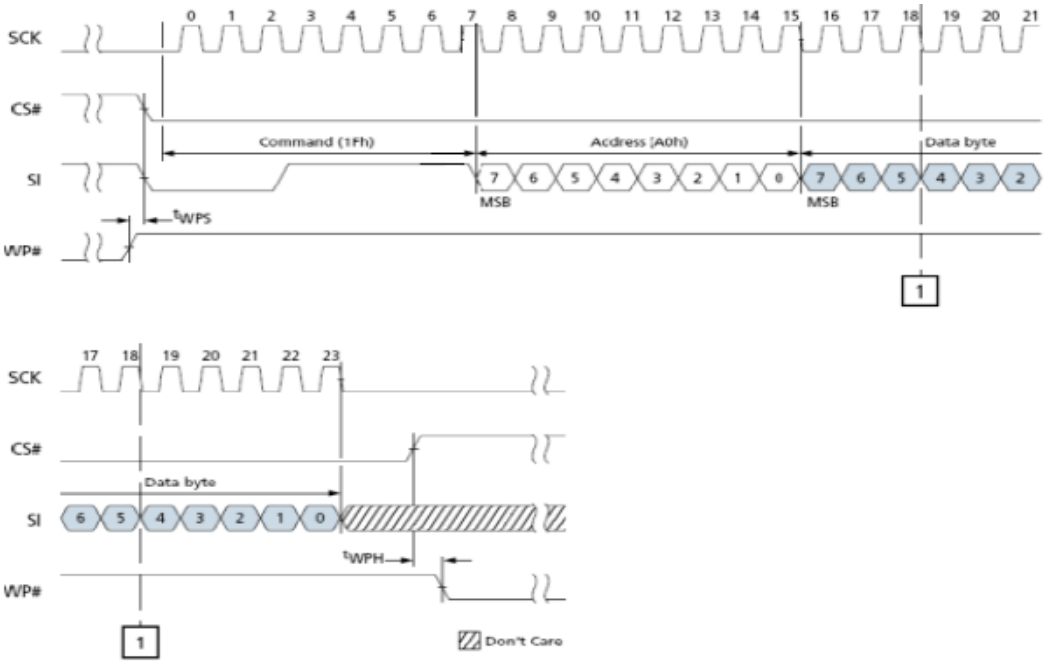
Hold Mode and HOLD# Timing

HOLD# pin provides a method to pause serial communication with the device but doesn't terminate any READ, PROGRAM, or ERASE operation currently in progress.

Hold mode starts at the falling edge of HOLD# provided SCK is also Low. If SCK is high when HOLD# goes Low, hold mode begins after the next falling edge of SCK. Similarly, hold mode is exited at the rising edge of HOLD# provided SCK is also Low. If SCK is High, hold mode ends after the next falling edge of SCK. During hold mode, SO is Hi-Z, and SI and SCK inputs are ignored.



HOLD# Timing



WP# Timing

COMMAND SET

Function	Op Code	Address Byte	Dummy Byte	Data Bytes
BLOCK ERASE	D8h	3	0	0
GET FEATURE(1)	0Fh	1	0	1
SET FEATURE	1Fh	1	0	1
WRITE DISABLE	04h	0	0	0
WRITE ENABLE	06h	0	0	0
PROGRAM LOAD	02h	2	0	1 to 2176
PROGRAM LOAD x4(2)	32h	2	0	1 to 2176
PROGRAM LOAD RANDOM DATA	84h	2	0	1 to 2176
PROGRAM LOAD RANDOM DATA x4(2)	34h	2	0	1 to 2176
PROGRAM EXECUTE	10h	3	0	0
PAGE READ	13h	3	0	0
READ FROM CACHE	03h, 0Bh	2	1	1 to 2176
READ FROM CACHE with 4Byte Address	0Ch	2	3	1 to 2176
READ FROM CACHE x2(3)	3Bh	2	1	1 to 2176
READ FROM CACHE x2 with 4Byte Address(3)	3Ch	2	3	1 to 2176
READ FROM CACHE x4(2)	6Bh	2	1	1 to 2176
READ FROM CACHE x4 with 4Byte Address(2)	6Ch	2	3	1 to 2176
FAST READ X2 IO(4)	BBh	2	1	1 to 2176
FAST READ X2 IO with 4Byte Address(4)	BCh	2	3	1 to 2176
FAST READ X4 IO (4)	EBh	2	2	1 to 2176
FAST READ X4 IO with 4Byte Address (4)	ECh	2	5	1 to 2176
READ ID	9Fh	1	0	2
RESET	FFh	0	0	0
DEEP POWER DOWN entry	B9h	~~0~~	0	0
DEEP POWER DOWN exit	ABh	0	0	0
CACHE READ	31h	0	0	0
LAST PAGE CACHE READ	3Fh	0	0	0
CACHE READ RANDOM PAGE	30h	3	0	0

Note:
1. Refer to Feature Register.
2. Command/Address is 1-bit input per clock period, data is 4-bit input/output per clock period.
3. Command/Address is 1-bit input per clock period, data is 2-bit output per clock period.
4. Command is 1-bit input per clock period & Address is 2/4-bit input per clock period, data is 2/4-bit output per clock period.

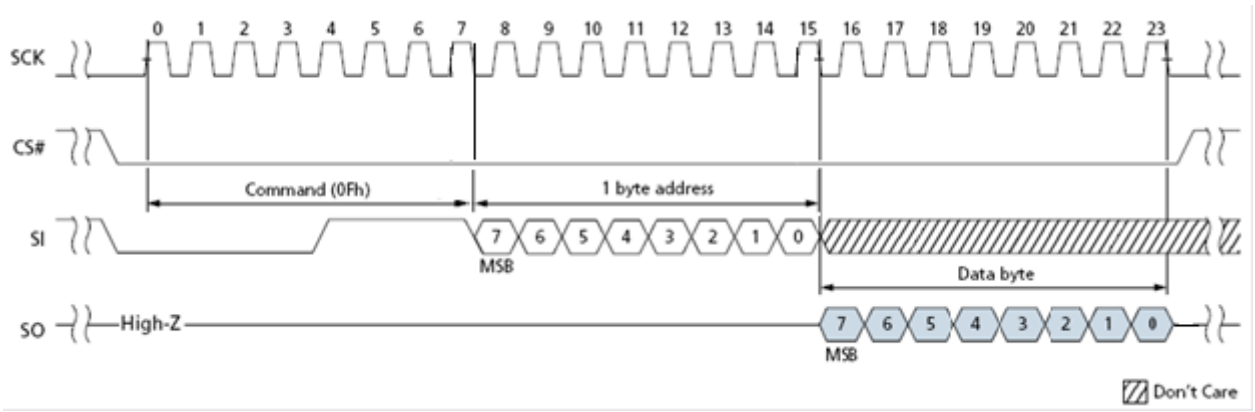
Feature Operations

Feature Registers are Protection Register (PR), Configuration Register (CR) & Status Register (SR). Each Feature Register is accessed by the GET FEATURE (0Fh) and SET FEATURE (1Fh) commands are used to alter the device behavior from the default power-on behavior. These commands use a 1-Byte feature address to determine which feature is to be read or modified.

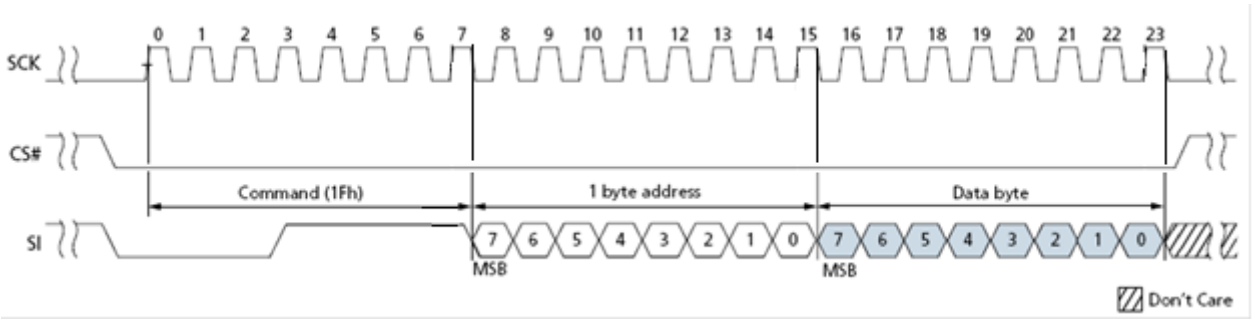
When a feature is set, it remains active until the device is power cycled or the feature is written to. Unless otherwise specified in the Table below, once the device is set, it remains set, even if a RESET (FFh) command is issued.

Feature Settings Table

Register	Acronym	Address	Data Bits							
			7	6	5	4	3	2	1	0
Protection Register	PR	A0h	BPRWD	BP3	BP2	BP1	BP0	T/B-P	WP-E	SP
Configuration Register	CR	B0h	OTP-P	OTP-E	PR-L	ECC-E	Reserved	Reserved	Reserved	HD
Status Register	SR	C0h	Reserved	ECC_S2	ECC_S1	ECC_S0	P_Fail	E_Fail	WEL	OIP
Output Driver Register	ODR	D0h	Reserved	DRV_S1	DRV_S0	Reserved	Reserved	Reserved	Reserved	Reserved



GET FEATURE (0Fh) Timing



SET FEATURE (1Fh) Timing

Protection Resister (PR, A0h)

Protection Register Setting

A0h	Data Bits							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Definition	Block Protection Register Write Disable (BPRWD)	Block Protect 3 (BP3)	Block Protect 2 (BP2)	Block Protect 1 (BP1)	Block Protect 0 (BP0)	Top / Bottom Protect (TB-P)	WP# Enable (WP-E)	Solid Protection (SP)
Shipment default	0	1	1	1	1	1	0	0

Note:

1. All bits in A0h are volatile writable.
2. Once BP[3:0], T/B-P, and WP-E bits are set correctly, SP and BPRWD should both be set to “1” to lock the protection in the PR (Protection Register) until next Power cycle.
3. If BPRWD is enabled and WP# is LOW, then the block protection register (BP0~BP3 and TB-P) cannot be changed.
4. SP bit is for Solid-protection. Once the SP bit sets as 1, the rest of the protection bits (BPx bits, TB-P, WP-E bits) cannot be changed during the current power cycle.

Write Protection Enable Bit (WP-E)

The Write Protection Enable bit (WP-E) is a volatile read/write bits in the Protection register-1. The WP-E bit, in conjunction with SP (Solid Protection) & BPRWD (Block Protection Register Write Disable), controls the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection, WP# pin functionality, and Quad SPI operation enable/disable. When WP-E = 0 (default value), the device is in Software Protection mode, WP# & HOLD# pins are multiplexed as IO pins. When WP-E is set to 1, the device is in Hardware Protection mode, all Quad functions are disabled and WP# & HOLD# pins become dedicated control input pins.

Solid Protection and Block Protection Register Write Disable Bits (SP, BPRWD)

The Solid Protection and Protection Register Disable Bits (SP, BPRWD) are volatile read/write bits in the Protection register -0 and -7. These two bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection.

Related Protection Bits of Protection Register

Software Protection (Controller, X4 Program/ Read is enable)				
BPRWD (7)	WP-E (1)	SP (0)	WP#/ IO2	**Description**
0	0	0	X	No WP# functionality, and WP# pin will always function as IO2
1	0	0	0	PR cannot be changed, and WP# pin will always function as IO2
1	0	0	1	PR can be changed, and WP# pin will always function as IO2
0	0	1	X	PR is locked until next Power cycle, WP# pin will function as IO2
1	0	1	X	Set PR-L=1 is allowed , PR is locked until next Power cycle, WP# pin will function as IO2
Hardware Protection (System Circuit/ PCB layout, X4 Program/ Read is disable)				
BPRWD (7)	WP-E (1)	SP (0)	WP# only	**Description**
X	1	0	V_{CC}	PR can be changed
0	1	1	V_{CC}	PR is locked until next Power cycle
1	1	1	V_{CC}	Set PR-L=1 is allowed, PR is locked until next Power cycle
X	1	X	V_{SS}	All Write operations are blocked, and entire device (Register, Array, and OTP area) is Read-only

Note:

1. PR means Protection Register.
2. When SP = “1” and BPRWD = “0”, a cycle of power-down to power-up will change the state to SP = “0” and BPRWD = “0”

Block Protection Operation (BP0~BP3, T/B-P)

Blocks can be locked to prevent Program and Erase operations. The users set the range of protection blocks as the entire device or a portion of the device using the BP0~BP3 bits (bits [6:3]) in the Feature operation address A0h. The users set the Block Protection bits by the Set Feature Operation. After the power on sequence, all Block Protection Bits are locked (bits [6:3] are all set to 1).

If the Program Execute (10h) or Block Erase (D8h) command is issued to the protection blocks, Program Fail or Erase Fail (P-Fail ot E_Fail) will be indicated Feature table.

The users must clear / change the Block Protection bits using Set Feature command to unlock the entire of the device or portion of the device. When BPRWD bit is enable and WP # pin is Low, the users cannot switch Block Protection bits (BP0~BP3 and TB-P).

Block Protect Bits of Protection Register

BP3 (6)	BP2 (5)	BP1 (4)	BP0 (3)	T/B-P (2)	Protected Blocks
0	0	0	0	X	None; all unlocked
0	0	0	1	0	Upper 1/1024 locked (2046：2047)
0	0	1	0	0	Upper 1/512 locked (2044：2047)
0	0	1	1	0	Upper 1/256 locked (2040：2047)
0	1	0	0	0	Upper 1/128 locked (2032：2047)
0	1	0	1	0	Upper 1/64 locked (2016：2047)
0	1	1	0	0	Upper 1/32 locked (1984：2047)
0	1	1	1	0	Upper 1/16 locked (1920：2047)
1	0	0	0	0	Upper 1/8 locked (1792：2047)
1	0	0	1	0	Upper 1/4 locked (1536：2047)
1	0	1	0	0	Upper 1/2 locked (1024：2047)
0	0	0	1	1	Lower 1/1024 locked (0：1)
0	0	1	0	1	Lower 1/512 locked (0：3)
0	0	1	1	1	Lower 1/256 locked (0：7)
0	1	0	0	1	Lower 1/128 locked (0：15)
0	1	0	1	1	Lower 1/64 locked (0：31)
0	1	1	0	1	Lower 1/32 locked (0：63)
0	1	1	1	1	Lower 1/16 locked (0：127)
1	0	0	0	1	Lower 1/8 locked (0：255)
1	0	0	1	1	Lower 1/4 locked (0：511)
1	0	1	0	1	Lower 1/2 locked (0：1023)
1	1	X	X	X	All locked
All Others					All locked

Note:
1. X = don't care
2. Any Erase or Program command for the protected area will be ignored.

Configuration Register (CR, B0h)

Configuration Register Setting

B0h	Data Bits							
Bit	7	6	5	4	3	2	1	0
Definition	OTP Pages Protect (OTP-P)	OTP Pages Enable(1) (OTP-E)	Protection Register Lock (PR-L)	ECC Enable(2) (ECC-E)	Reserved	Reserved	Reserved	HD
Shipment default	0	0	0	1	0	0	0	0

Note:
1. To Program/ Read OTP area, OTP-E must be set to "1".
2. 8-bit internal ECC for all READ and PROGRAM operations can be enabled (ECC enable = 1) or disabled (ECC enable = 0). The internal ECC is enabled after the power on sequence. The users switch the ECC-E bit (bit [4]) in address B0h of the feature table to enable or disable the internal ECC. The users set or clear a bit by the Set Feature command. If the ECC-E bit is cleared to 0 in the feature table, internal ECC will be disabled. In this case, the spare area size is changed from 64 bytes to 128 bytes automatically. When the users switching the ECC-E bit, the users must issue the Set Feature command just before the Page Read Operation, Page Program Operation or Block Erase Operation.

One Time Program Protect Bit (OTP-P)

OTP area stores critical data that cannot be changed once it's locked. The OTP area consists of 30 pages of 2,112-Byte each (When ECC is enable). Only Program command can be issued to the OTP area to change the data from "1" to "0", and data is not reversible ("0" to "1") by the Erase command. Once the correct data is programmed in and verified, the system developer can set OTP-P bit to 1, so that the entire OTP area will be locked to prevent further alteration to the data.

OTP Access Mode Enable Bit (OTP-E) – Volatile Writable

The OTP-E bit must be set to 1 in order to use the standard Program/Read commands to access the OTP area as well as to read the Unique ID / Parameter Page information. The default value after power up or a RESET command is 0.

Protection Register Lock Bit (PR-L) – OTP lockable

The PR-L lock bit is used to OTP lock the values in the Protection Register (PR). Depending on the settings in the PR, the device can be configured to have a portion of or up to the entire array to be write-protected, and the setting can be OTP locked by setting PR-L bit to 1. PR-L bit can only be set to 1 when SP & BPRWD are set to (1,1).
Once the BP0~3, T/BP, WPE bits are set correctly, SP and BPRWD should also be set to "1"s as well to allow PR-L bit being set to "1" to lock the protection settings in the Protection Register (PR)

One time programmable (OTP) Operations

The device offers one-time programmable memory area. Thirty full pages of OTP data are available on the device, and the entire range is guaranteed to be good.

The OTP area leaves the factory in an unwritten state. The OTP area cannot be erased, whether it is protected or not. Protecting the OTP area prevents further programming of that area.

To access the OTP area, the user must issue the SET FEATURES command, followed by feature address B0h. When the OTP is ready to access, pages 00h-1Dh can be programed in ascending order. Please note that no partial-page program is allowed in the OTP area. A programmed OTP page will be automatically protected.

The PROGRAM LOAD (02h) and PROGRAM EXECUTE (10h) commands can be used to program the pages. Also the PAGE READ (13h) commands, READ FROM CACHE (03h / 0Bh / 0Ch/ 3Bh / 3Ch / 6Bh/ 6Ch) and FAST READ (BBh / BCh / EBh / ECh) commands can be used to read the OTP area.

Access OTP area

1. Issue Set Feature command (1Fh), and Issue the Feature address (B0h)
2. Set OTP Protect Bit Low (OTP-P) and OTP Enable(OTP-E) Bit High
3. Issue Program Load (02h)
4. Issue Program Execute (10h) command. Every page can program only once
5. Set OTP Enable Bit Low after access OTP area done

Protect OTP area

1. Issue Set Feature command (1Fh), and Issue the Feature address (B0h)
2. Set OTP Protect Bit (OTP-P) High and OTP Enable Bit High
3. Issue Program Execute command (10h) for OTP area protected
4. Set OTP Protect Bit (OTP-P) Low and OTP Enable Bit (OTP-E) Low after protect OTP area done

OTP Area Information

There are 30 pages of OTP Area. Among these pages, one is for Unique ID Page, another one is Parameter Page.

Logical Address	Description
00h	Unique ID page
01h	Parameter page
02h~1Dh	Regular OTP pages

OTP Address mapping table

OTP Protect Bit (7)	OTP Enable Bit (6)	State
0	0	Normal operation (read array)
0	1	Access OTP area
1	0	Not applicable
1	1	Lock the OTP area

OTP State Bits of Configuration Register

Hold Disable Bit (HD)

When WP-E is “0”, during the Program Load x4 operation (32h/34h), to prevent accidental operation from host to place the Hold Input (drive Hold# low), Hold Disable (HD) can be set by SET Feature (B0h, 0Bit).

While HD bit is "0" (default), during the Program Load x4 operation, HOLD# function still can be enabled before data arriving SI0-3. HD bit is allowed to be set “1” only when WP-E bit is “0”. While WP-E bit is “0” and HD bit is set "1", Hold Input function as well as WP# control function are disabled. HD bit returns to “ 0” after next power cycle.

Parameter Page Data Definitions

The table below lists all the key data byte locations. All other unspecified byte locations have 00h data as default.

Parameter Page Data Structure

Byte	Description	Value
0-3	Parameter page signature ("O", "N", "F", "I")	4Fh, 4Eh, 46h, 49h
4-5	Revision number	00h, 00h
6-7	Features supported	00h, 00h
8-9	Optional commands supported	06h, 00h
10-31	Reserved	All 00h
32-43	Device manufacturer	50h, 4Fh, 57h, 45h, 52h, 43h, 48h, 49h, 50h, 20h, 20h, 20h
44-63	Device mode	50h, 53h, 52h, 32h, 47h, 53h, 32h, 30h, 44h, 4Eh, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	Manufacturer ID	C8h
65-66	Date code	00h, 00h
67-79	Reserved	All 00h
80-83	Number of data bytes per page	00h, 08h, 00h, 00h
84-85	Number of spare bytes per page	80h, 00h
86-89	Number of data bytes per partial page	00h, 02h, 00h, 00h
90-91	Number of spare bytes per partial page	20h, 00h
92-95	Number of pages per block	40h, 00h, 00h, 00h
96-99	Number of blocks per unit	00h, 08h, 00h, 00h
100	Number of logical units	01h
101	Number of address cycles	00h
102	Number of bits per cell	01h
103-104	Number of maximum bad blocks per unit	28h, 00h
105-106	Block endurance	06h, 04h
107	Guaranteed valid blocks at beginning of target	01h
108-109	Block endurance of guaranteed valid blocks	00h, 00h
110	Number of partial programs per page	04h
111	Partial programming attributes	00h
112	Number of bits ECC	00h
113	Number of Interleaved address bits	00h
114	Interleaved operation attributes	00h
115-127	Reserved	All 00h
128	I/O pin capacitance	08h
129-132	Reserved	All 00h
133-134	tPROG (max)	84h, 03h
135-136	tBERS (max)	10h, 27h

137-138	tR (max)	82h, 00h
139-140	Reserved	All 00h
141-163	Reserved	All 00h
164-165	Vendor-specific revision number	00h, 00h
166-179	Reserved	All 00h
180-253	Reserved	All 00h
254-255	Integrity CRC	Set at test
256-511	Values of bytes 0-255	Values of bytes 0-255
512-767	Values of bytes 0-255	Values of bytes 0-255
768+	Additional redundant parameter pages	

Status Register (SR, C0h)

Software can read status register during the NAND device operation by issuing GET FEATURE (0Fh) command, followed by the feature address C0h. The status register will output the status of the operation, refer to Table below.

Status Register Setting

C0h	Data Bits							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Definition	Reserved	ECC_Status2	ECC_Status1	ECC_Status0	Program_Fail	Erase_Fail	Write Enable Latch	Operation In Progress
Shipment default	0	0	0	0	0	0	0	0

Bits of Status Register

Bit Name	Mode	Description
Program fail (Bit 3)	R	P_Fail is set to 1 as a program failure has occurred. P_Fail = 1 will also be set if the user attempts to program an invalid address or a locked region. P_Fail is set to 0 during the PROGRAM EXECUTE command sequence or the RESET command.
Erase fail (Bit 2)	R	E_Fail is set to 1 as an erase failure has occurred. E_Fail = 1 will also be set if the user attempts to erase a locked region, or if ERASE operation fails. E_Fail is set to 0 at the start of the BLOCK ERASE command sequence or the RESET command.
Write enable latch (Bit1)	W	This bit indicates the status of write enable/disable. 0: Write Disable (Default) 1: Write Enable WEL must be set to 1 to indicate the current status of the write enable, prior to issuing PROGRAM EXECUTE or BLOCK ERASE command. It is set by issuing WRITE ENABLE (06h) command. WEL is disabled (WEL=0) by issuing the WRITE DISABLE command (04h).
Operation in progress (Bit 0)	R	OIP is set to 1 when the device is busy; it means a PROGRAM EXECUTE, PAGE READ, BLOCK ERASE, CACHE READ, LAST PAGE CACHE READ or RESET command is executing. OIP is cleared to 0 as the interface is in ready state.
ECC_Status0 (Bit 4) ECC_Status1 (Bit 5) ECC_Status2 (Bit 6)	R	ECC_S is set to 00h either following a RESET, or at the beginning of the READ. It is then updated after the device completes a valid READ operation. The ECC Status bits values are don't care if ECC-E=0.

ECC Status Bits of Status Register

ECC_S2 (Bit6)	ECC_S1 (Bit5)	ECC_S0 (Bit4)	Description
0	0	0	No errors
0	0	1	1-3 bit error detected and corrected
0	1	0	9-bits or more than 9-bits errors detected and not corrected
0	1	1	4-6 bit error detected and corrected
1	0	1	7-8 bit error detected and corrected
1	0	0	Reserved
1	1	0	Reserved
1	1	1	Reserved

Output Driver Resister (DR, D0h)

Output Driver Register Setting

D0h	Data Bits							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Definition	Reserved	Driver_Strength1	Deiver_Strength0	Reserved	Reserved	Reserved	Reserved	Reserved
Shipment default	0	0	1	0	0	0	0	0

Driver Strength Bits of Output Driver Register

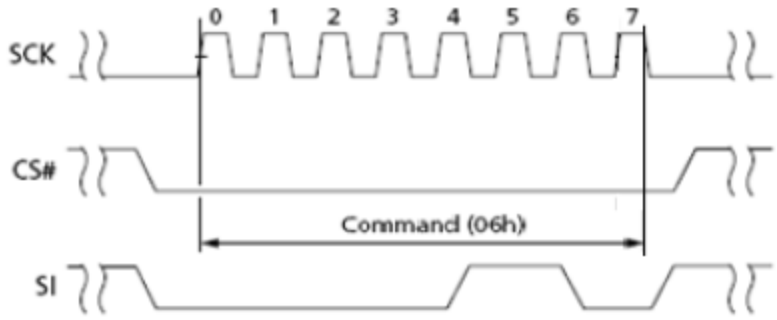
DRV_S1 (6)	DRV_S0 (5)	Driver Strength
0	0	100%
0	1	75%
1	0	50%
1	1	25%

Operations and Timing Diagrams

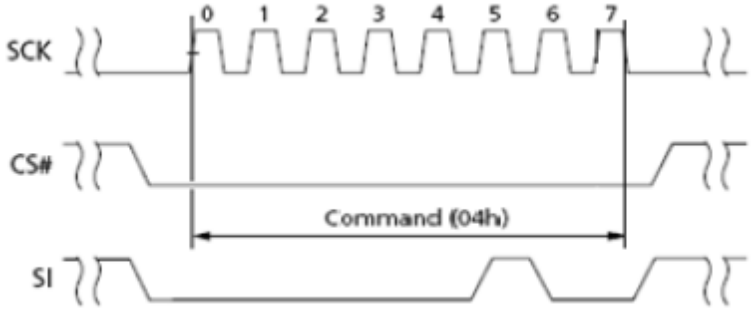
WRITE ENABLE and WRITE DISABLE (06h and 04h)

The WRITE ENABLE (06h) command sets the WEL bit (in status register) to 1. This is required in the following WRITE operations that change the contents of the memory array: PAGE PROGRAM, BLOCK ERASE, and OTP PROGRAM.

Contrarily, the WRITE DISABLE (04h) command sets the WEL bit to 0. This disables PAGE PROGRAM, BLOCK ERASE, and OTP PROGRAM.



WRITE ENABLE (06h) Timing



WRITE DISABLE (04h) Timing

PAGE READ (13h), READ FROM CACHE (03h or 0Bh) and Serial Output Timing

The command sequence is follows:

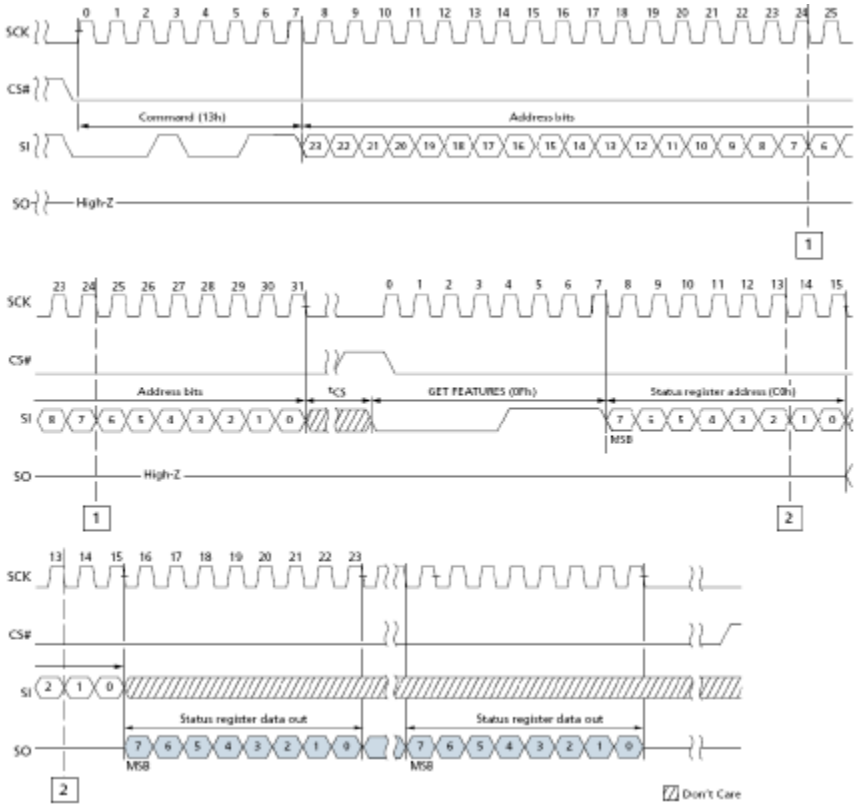
- 13h (PAGE READ to cache)
- 0Fh (GET FEATURE command to read the status)
- 0Bh or 03h (READ FROM CACHE x1) ; 0Ch (Read from CACHE x1 with 4 Bytes address)
  3Bh (READ FROM CACHE x2) ; 3Ch (Read from CACHE x2 with 4 Bytes address)
  6Bh (READ FROM CACHE x4) ; 6Ch (Read from CACHE x4 with 4 Bytes address)
  BBh (Fast Read x2 IO) ; BCh (Fast Read x2 IO with 4 Bytes address)
  EBh (Fast Read x4 IO) ; ECh (Fast Read x IO with 4 Bytes address)

PAGE READ (13h) command requires 24-bit address with 7 dummy and a 17-bit row address. After row address is registered, the device starts the transfer from the main array to the cache register, and is busy for tR time. During this time, GET FEATURE command can be issued to monitor the status of the operation. Following a status of successful completion, READ FROM CACHE command must be issued to read the data out of the cache.

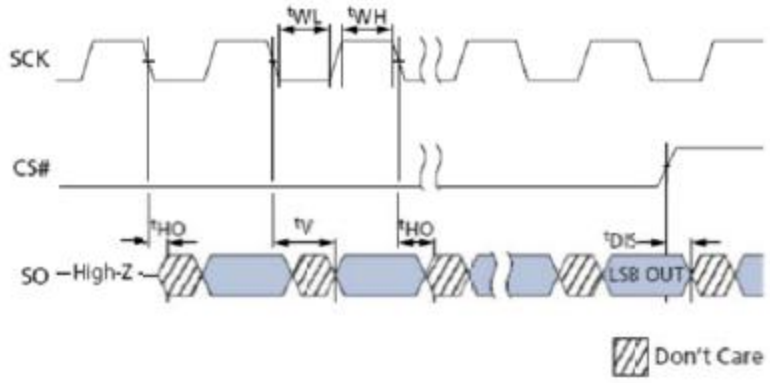
READ FROM CACHE (03h or 0Bh) command requires 16-bit address with 4 dummy bits and a 12-bit column address for the starting byte. The starting byte can be 0 to 2175, but after the end of the cache register is reached, the data does not wrap around and SO goes to a Hi-Z state.

BBh and BCh command allow for improved random access while maintaining two IO pins: SI and SO. It is similar to 3Bh command but with the capability to input Column Address or dummy clocks two bits per clock.

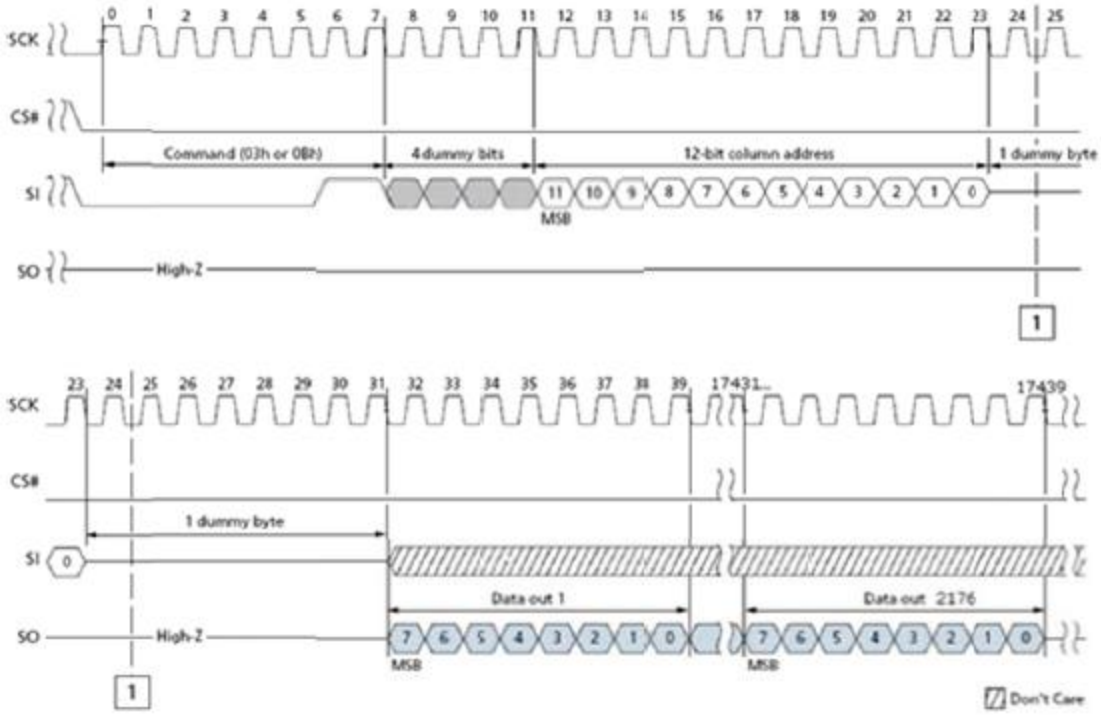
The data output sequence will start from the location specified by the Column Address input and continue to the end of the Page. Once the last byte of data is output, both SI (SO0) and SO (SO1) will become Hi-Z.



PAGE READ (13h) Timing



Serial Output Timing

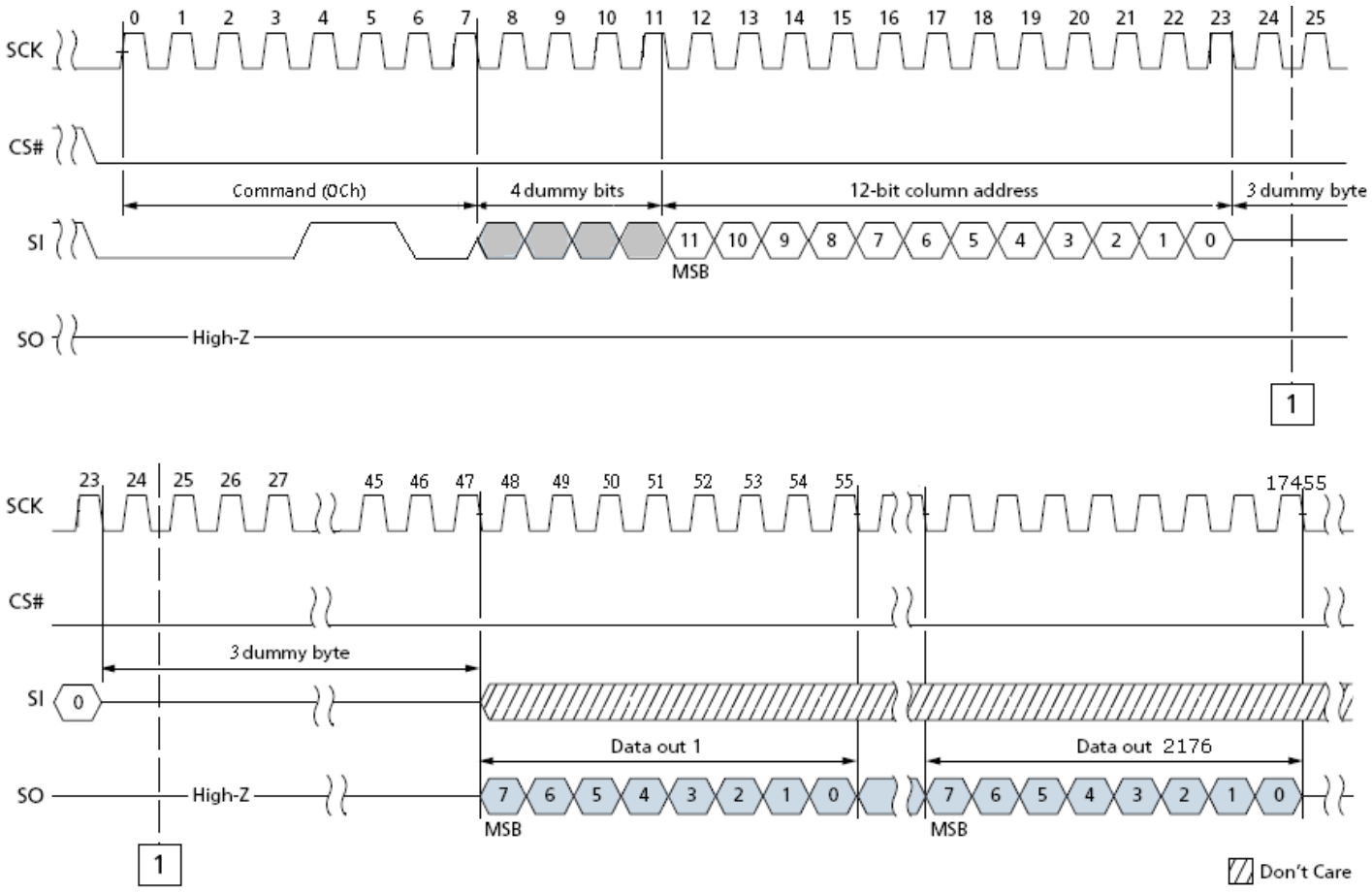


READ FROM CACHE (03h or 0Bh) Timing

Note:
When internal ECC is turned OFF, the maximum output data size is 2176 Bytes.

READ FROM CACHE with 4Byte Address (0Ch)

The Read from CACHE with 4 Byte address instruction allows one or more data bytes to be sequentially read from the Data Buffer after executing the Page Read instruction. The Read instruction is initiated by driving the CS# pin low and then shifting the instruction code "0Ch" followed by the 16-bit Column Address and 24-bit dummy clocks into the SI pin. After the address is received, the data byte of the addressed Data Buffer location will be shifted out on the SO pin at the falling edge of SCK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. The instruction is completed by driving CS# high.

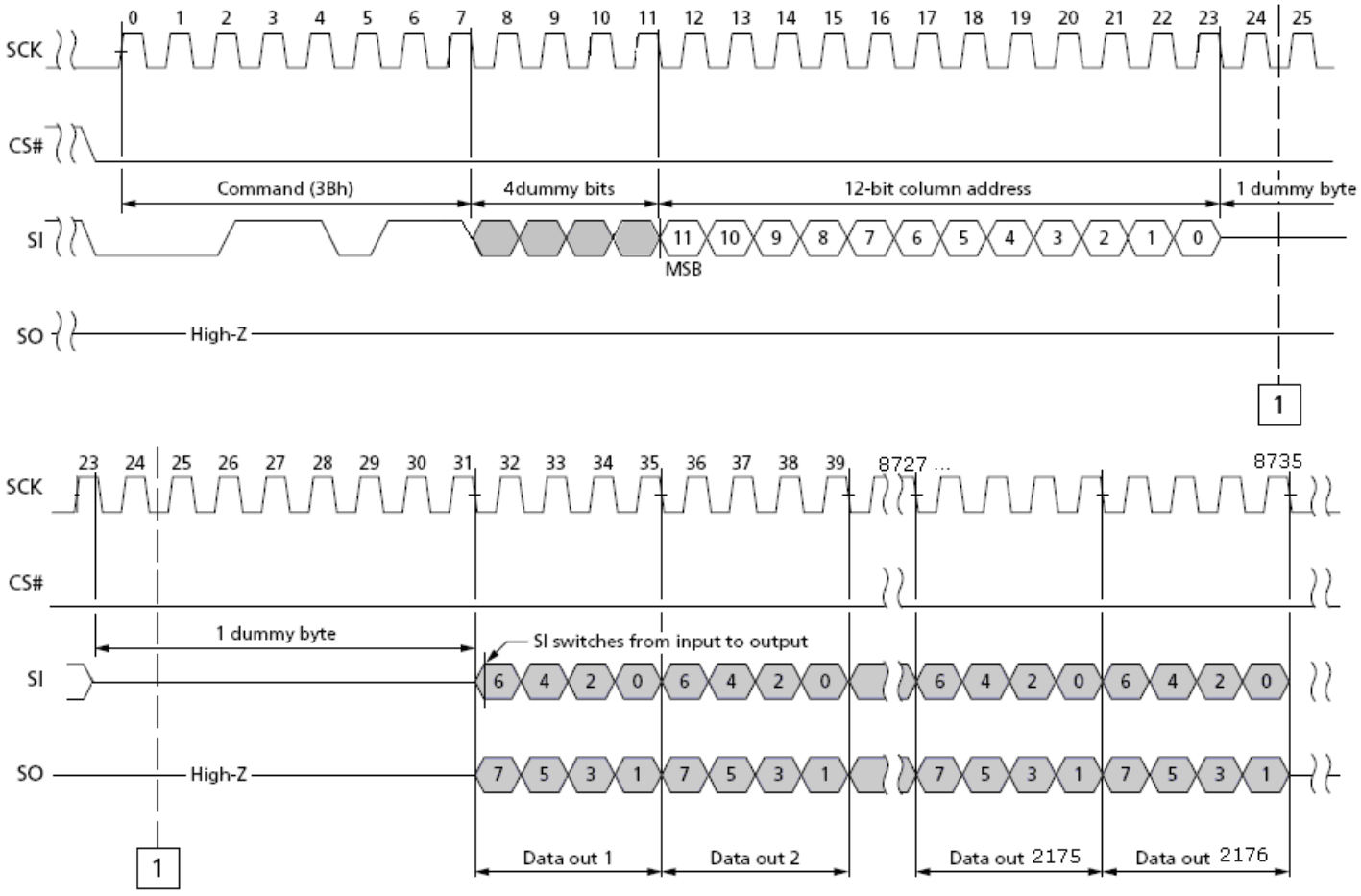


READ FROM CACHE with 4Byte Address (0Ch) Timing

READ FROM CACHE x2 (3Bh)

Read from CACHEx2 (3Bh) instruction is similar to the standard Read from CACHEx1 (0Bh) instruction except that data is output on two pins; SI (IO0) and SO (IO1). This allows data to be transferred at twice the rate of standard SPI devices.

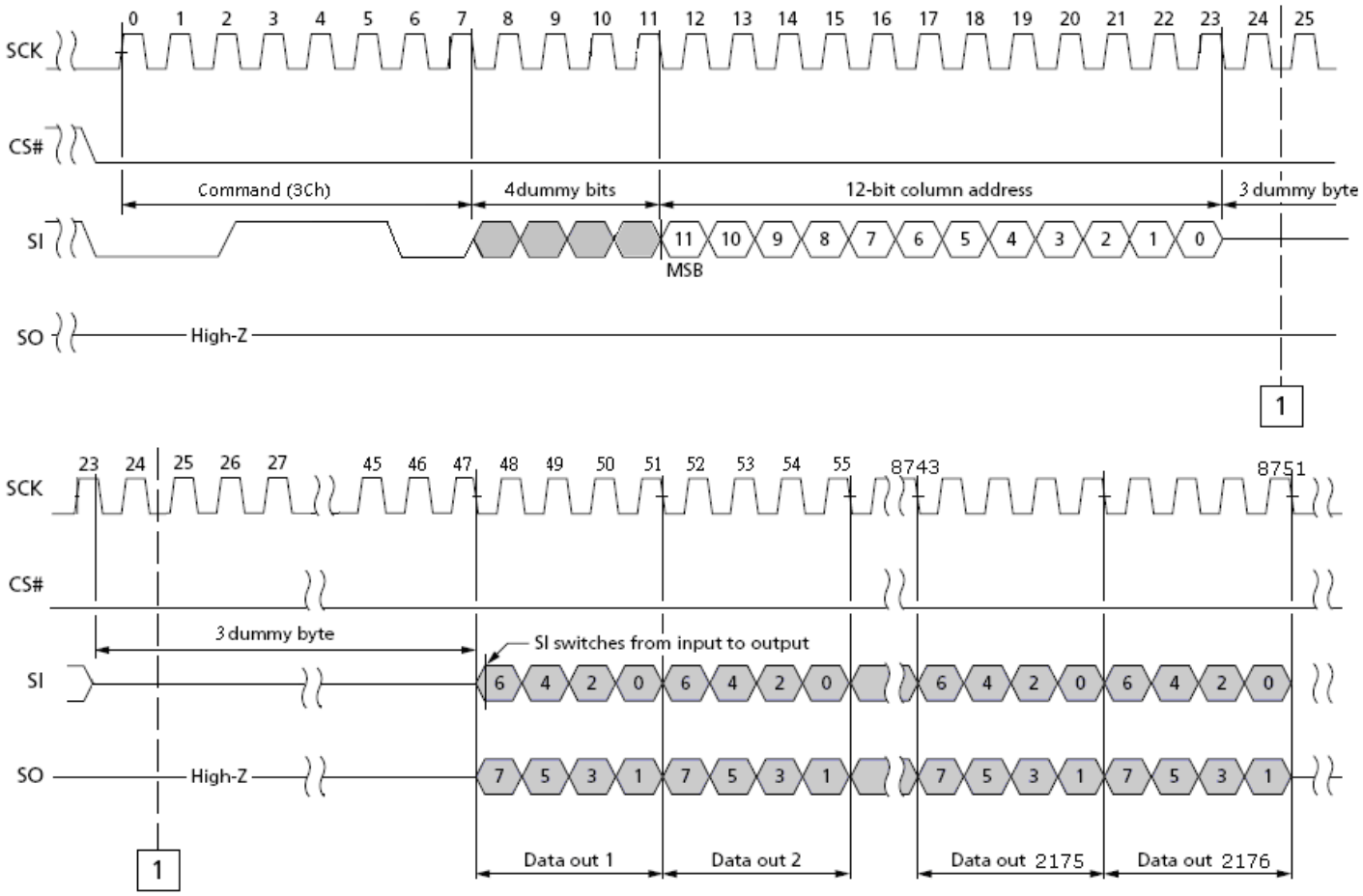
The Read from CACHE x2 data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.



READ FROM CACHE x2 (3Bh) Timing

READ FROM CACHE x2 with 4Byte Address (3Ch)

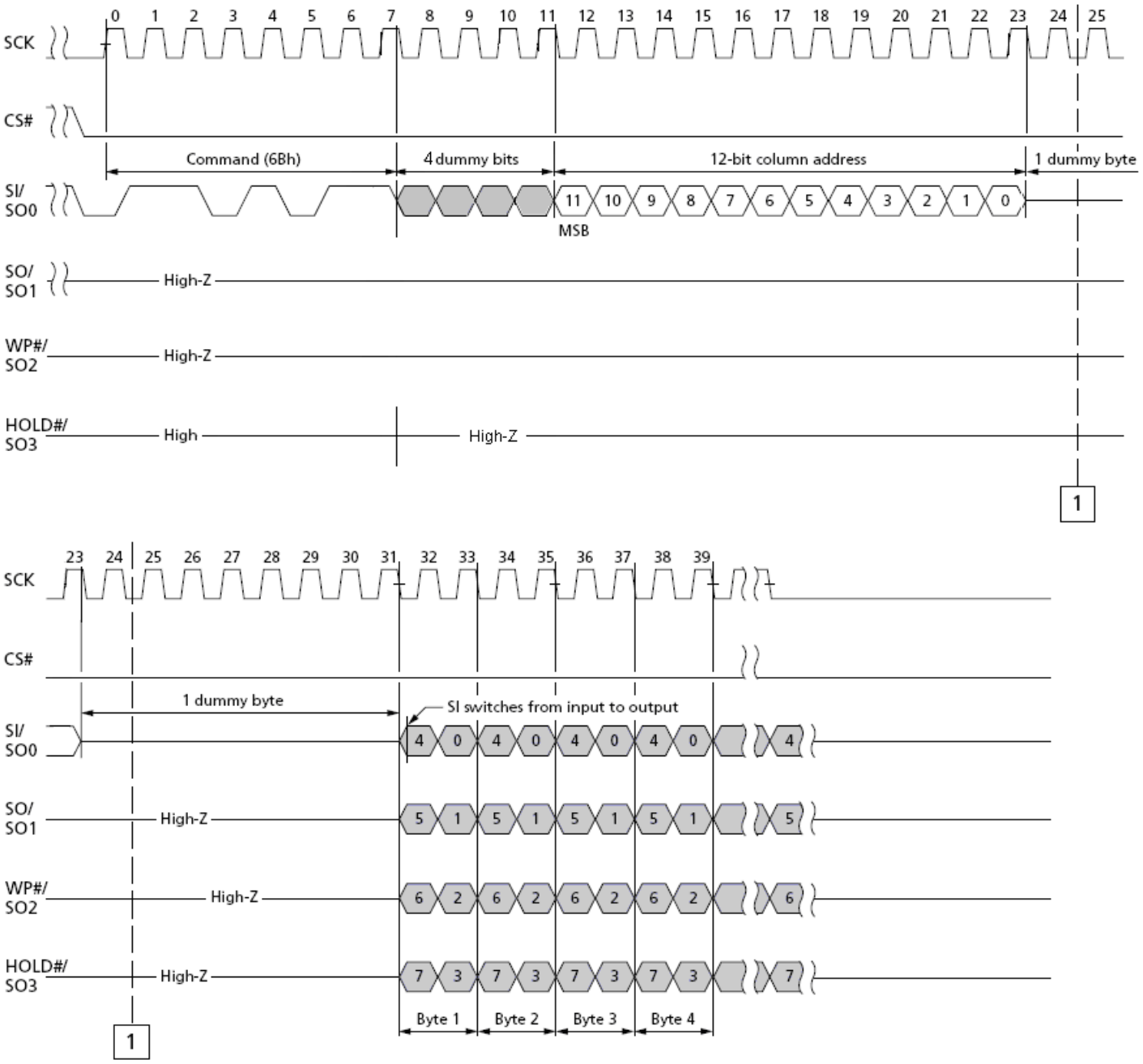
The Read from CACHEx2 with 4 Bytes address instruction is initiated by driving the CS# pin low and then shifting the instruction code "3Ch" followed by the 16-bit Column Address and 24-bit dummy clocks into the SI pin. After the address is received, the data byte of the addressed Data Buffer location will be shifted out on the SO and SI pin. Once the last byte of data is output, the output pin will become Hi-Z state.



READ FROM CACHE x2 with 4Byte Address (3Ch) Timing

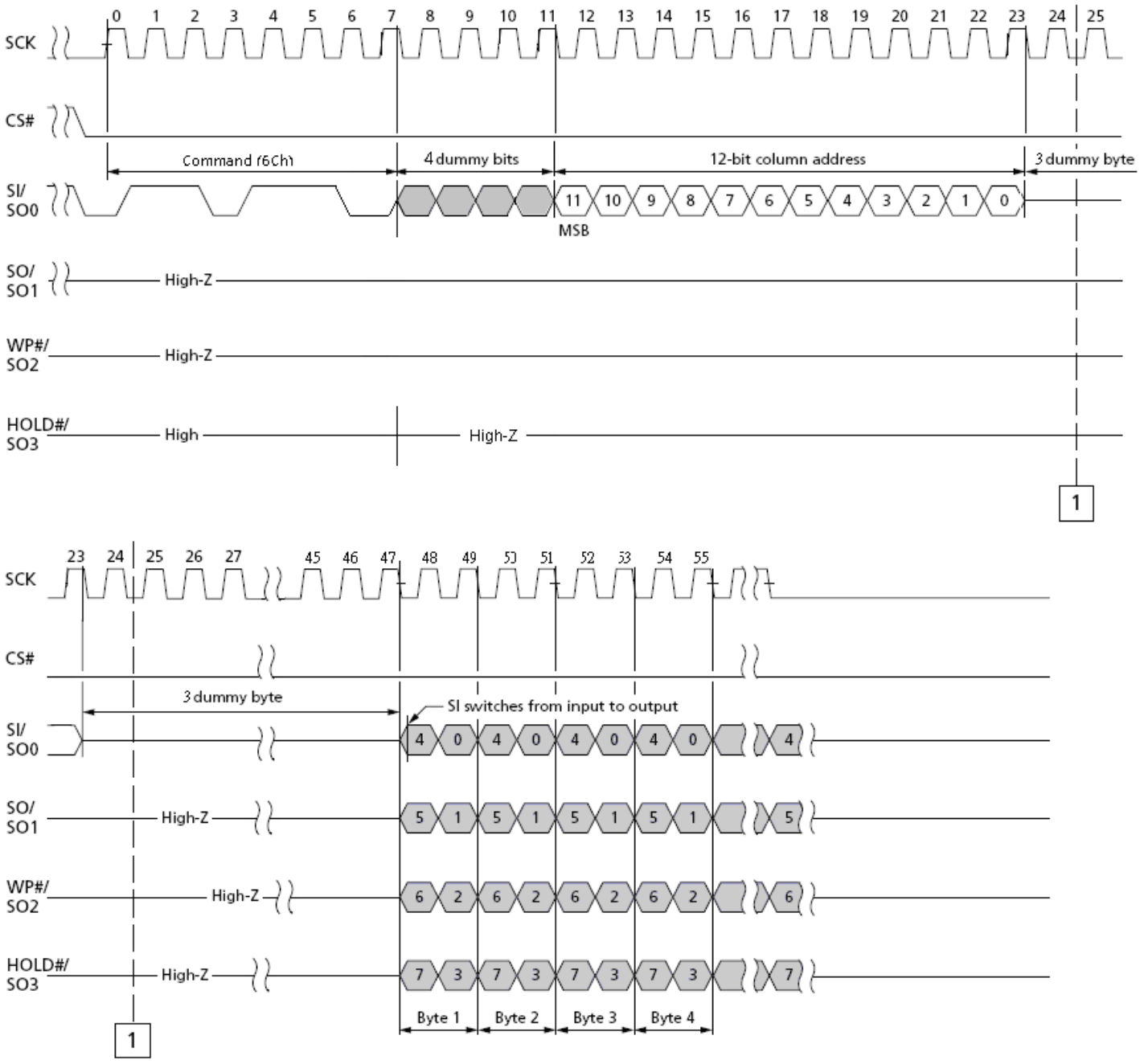
READ FROM CACHE x4 (6Bh)

Read from CACHEx4 (6Bh) instruction is similar to the standard Read from CACHEx2 (3Bh) instruction except that data is output on 4 pins; IO0, IO1, IO2 and IO3. This allows data to be transferred at twice the rate of standard SPI devices.



READ FROM CACHE x4 (6Bh) Timing

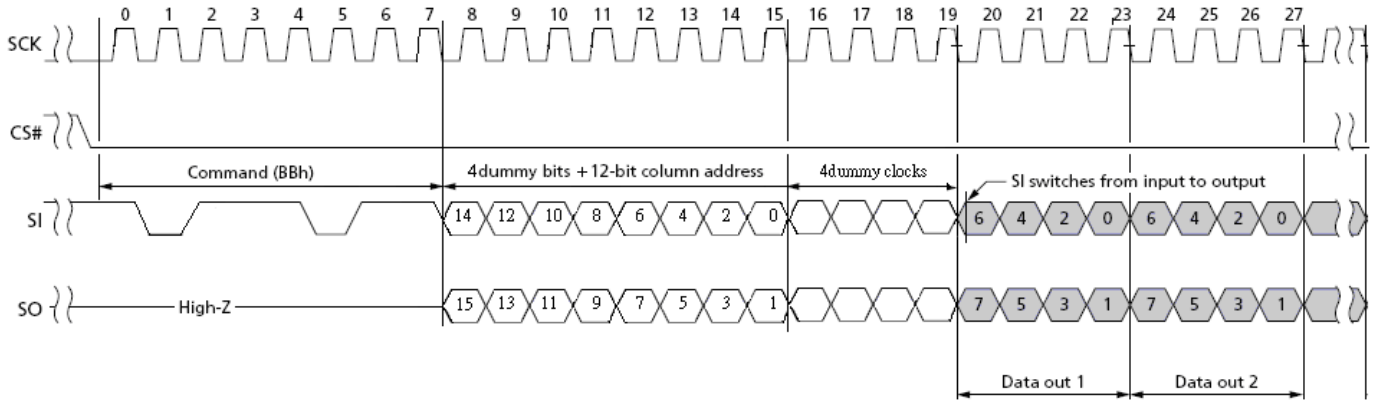
READ FROM CACHE x4 with 4Byte Address (6Ch)



READ FROM CACHE x4 with 4Byte Address (6Ch) Timing

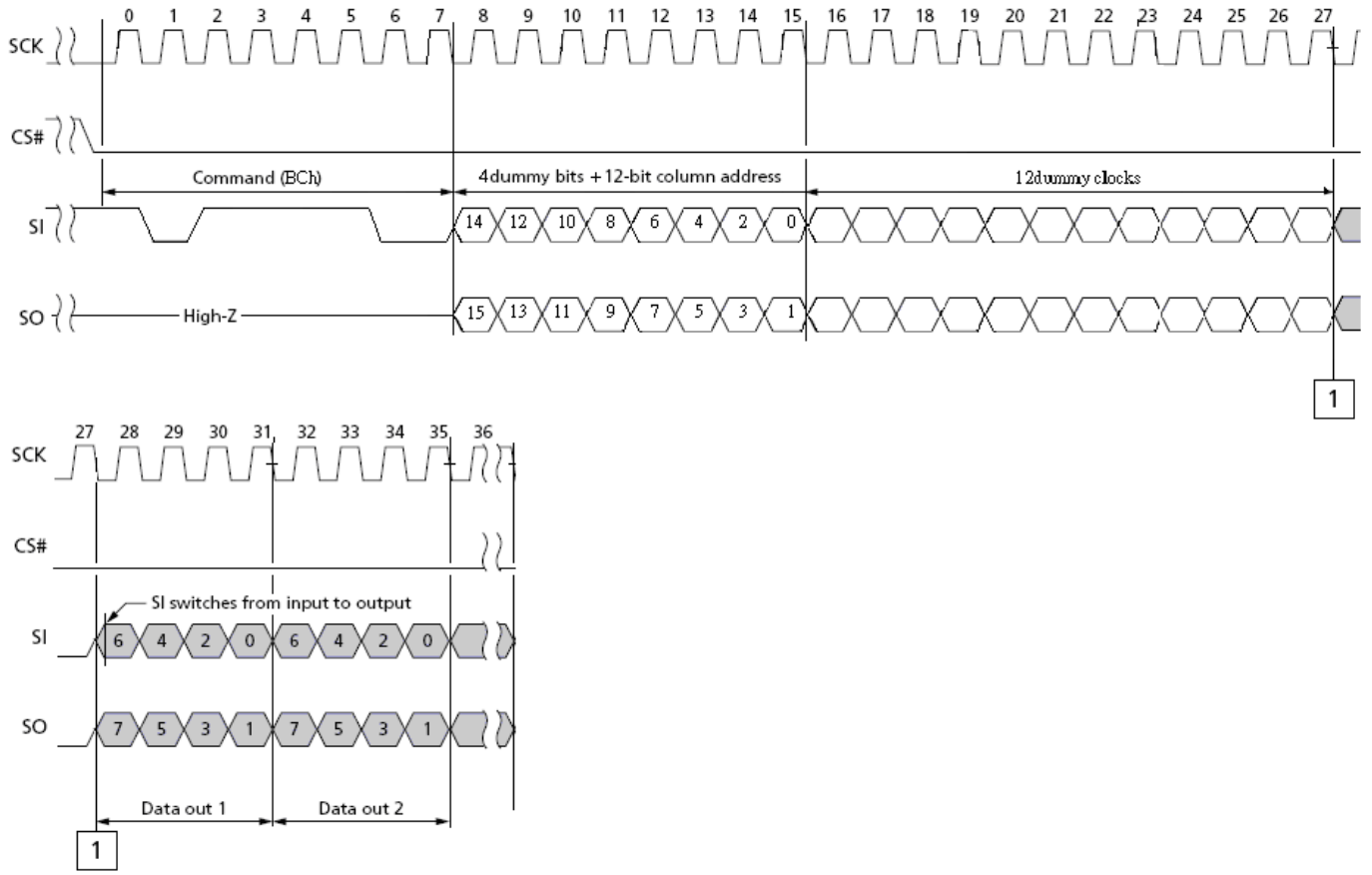
FAST READ x2 I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two IO pins, IO0 and IO1. It is similar to the Read from CACHEx2 (3Bh) instruction but with the capability to input the Column Address or the dummy clocks two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.



FAST READ x2 IO (BBh)

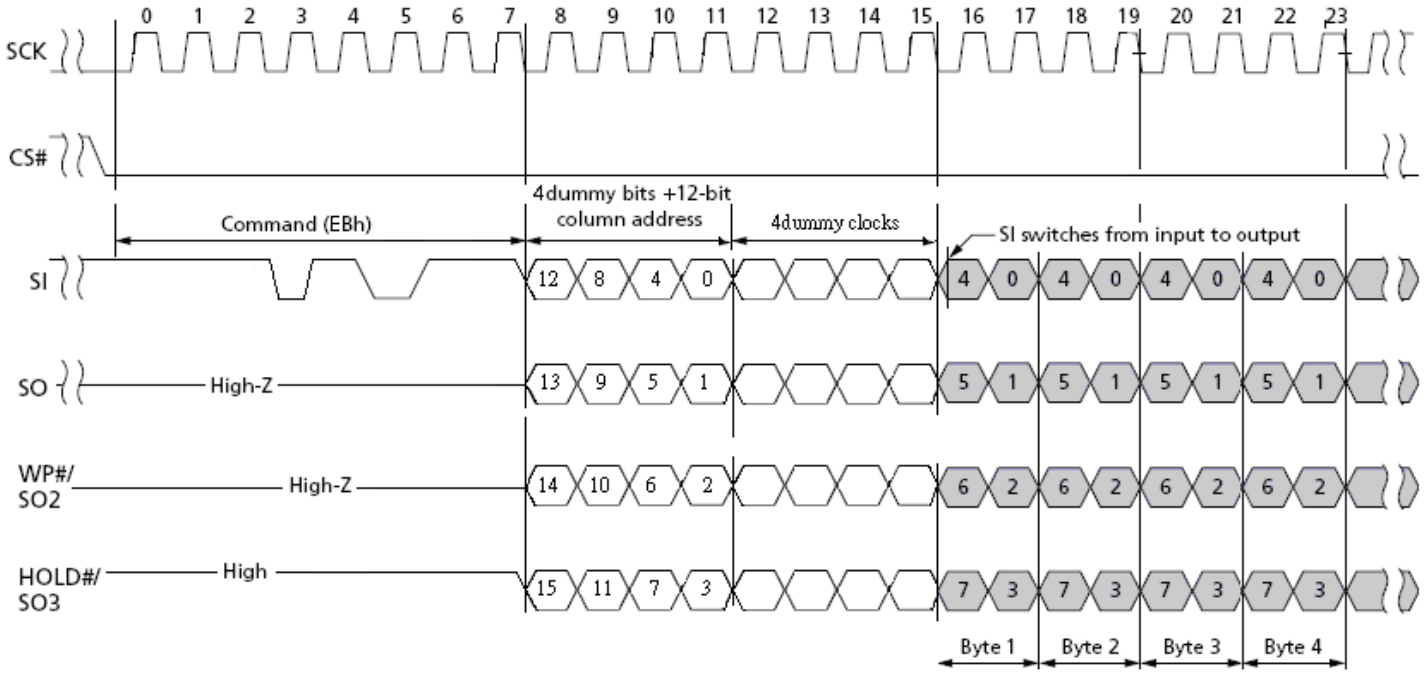
FAST READ x2 I/O with 4Bytes address (BCh)



FAST READ x2 IO with 4Byte Address (BCh)

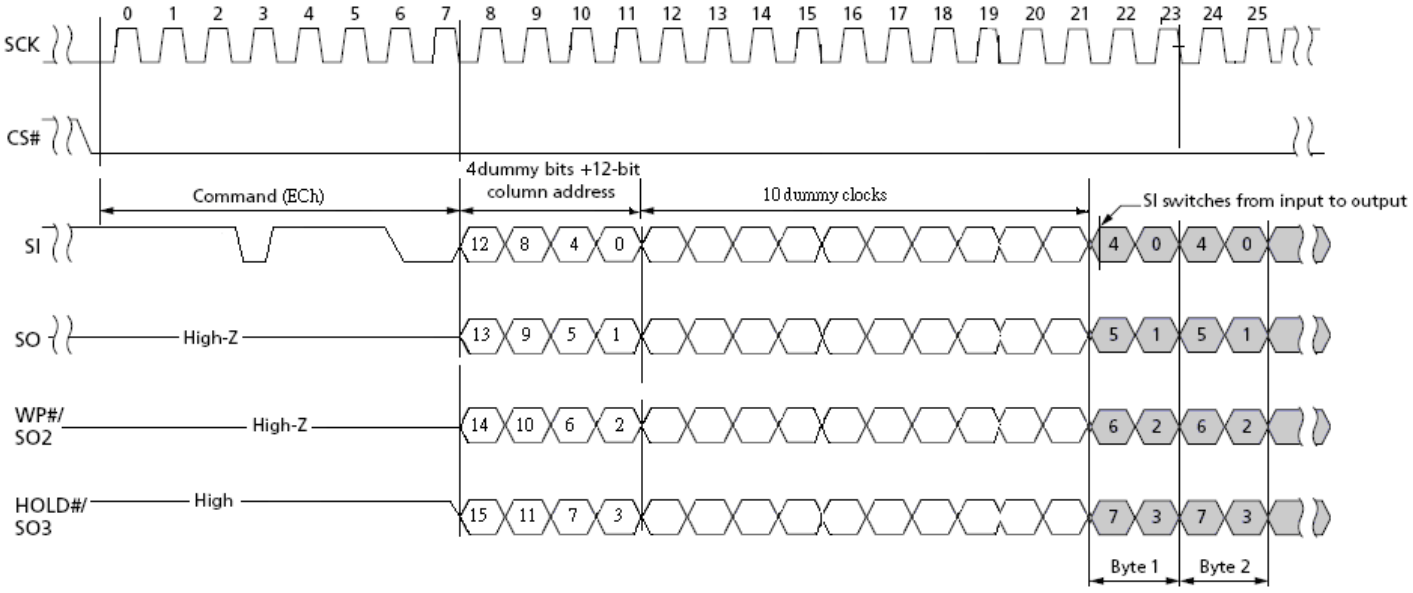
FAST READ x4 IO (EBh)

The Fast Read x4 IO (EBh) instruction, the address and data bits are input and output through four pins IO0, IO1, IO2 and IO3 prior to the data output, and with the capability to input data four bits per clock. The Quad I/O allows random access for code execution (XIP) directly from the Quad SPI.



FAST READ x4 IO (EBh)

FAST READ x4 IO with 4Bytes address (ECh)



Fast Read x4 IO with 4Byte Address (ECh)

PROGRAM LOAD (02h) operation

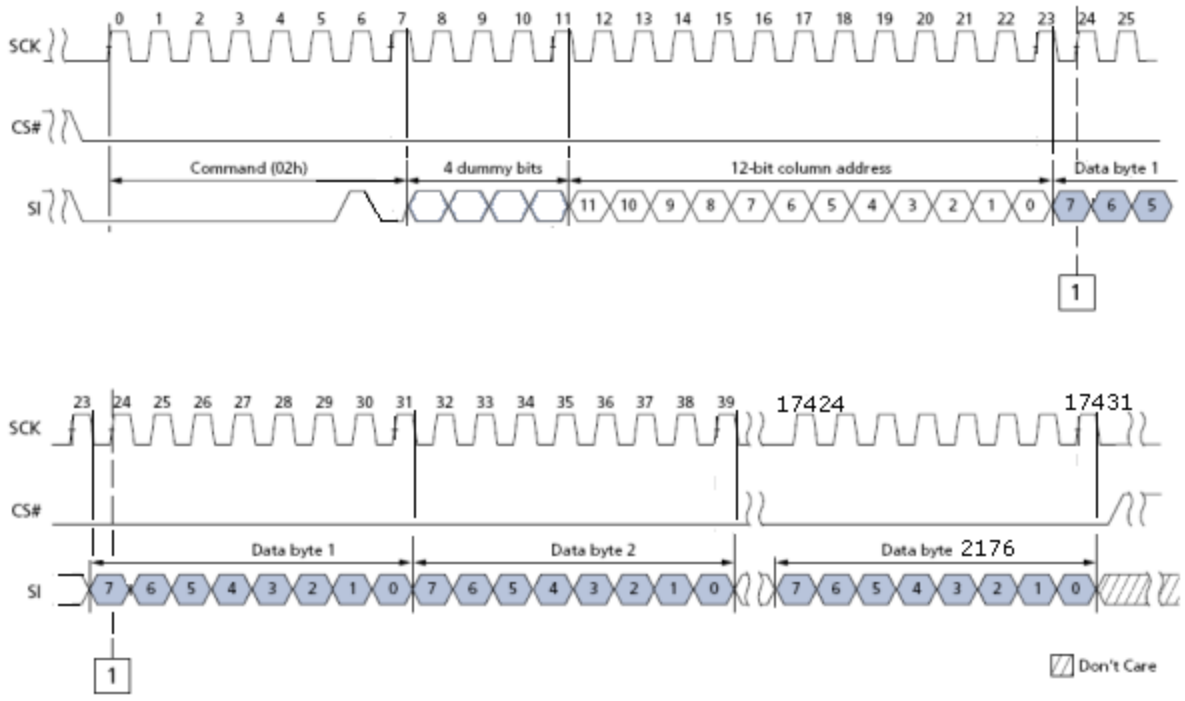
The command sequence is follows:

- 06h (WRITE ENABLE)
- 02h (PROGRAM LOAD x1) Or 32h (PROGRAM LOAD x4)
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

The page program operation sequence programs 1 byte to 2176 bytes of data within a page. If WRITE ENABLE command is not issued (WEL bit is not set), then the rest of the program sequence is ignored. PROGRAM LOAD command requires 16-bit address with 4 dummy and a 12-bit column address, then the data bytes to be loaded into cache register. Four partial page programs are allowed on a single page. If more than 2176 bytes are loaded, those additional bytes are ignored by the cache register.

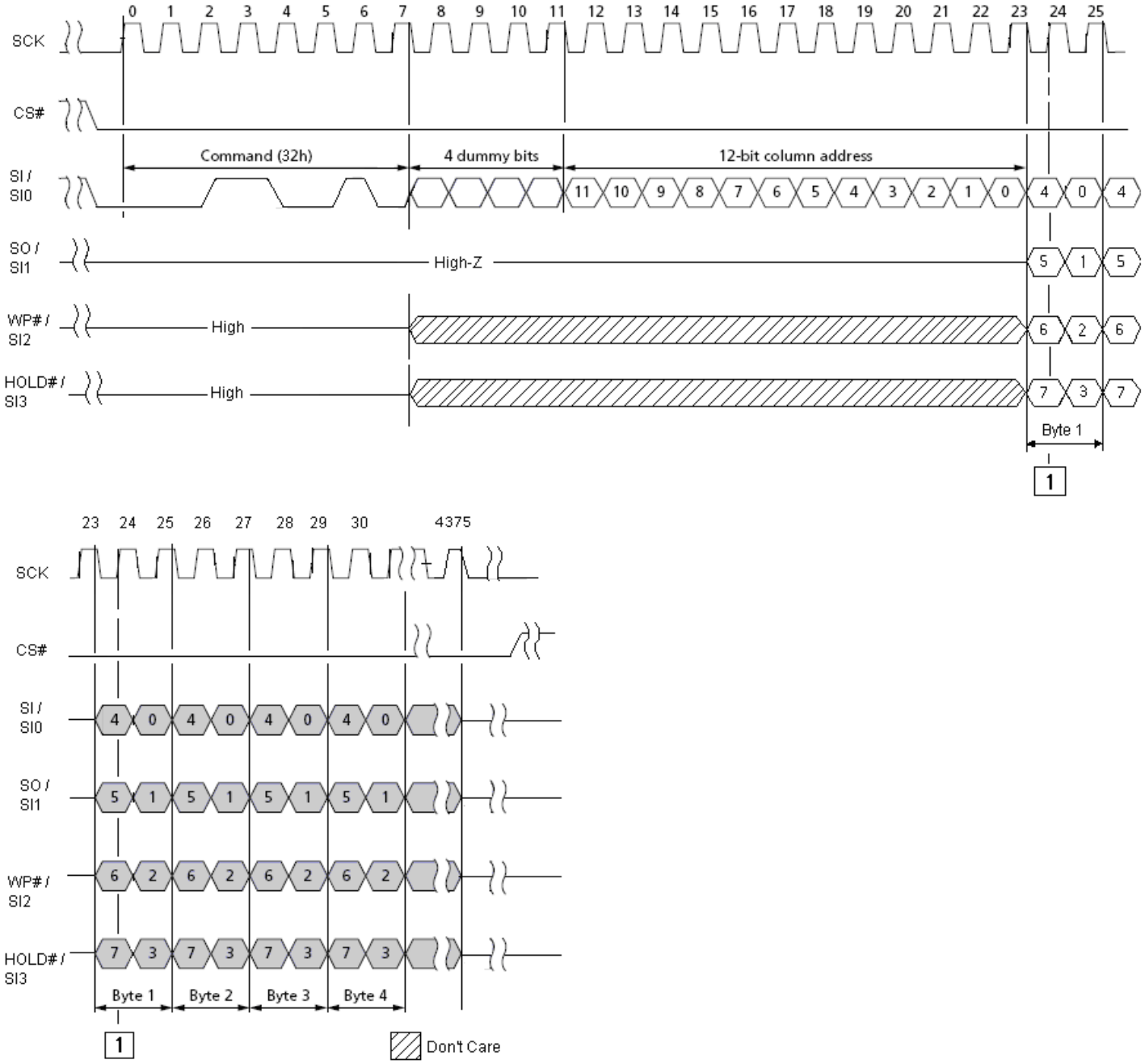
After the data is loaded, PROGRAM EXECUTE command must be issued to transfer the data from cache register to main array, and is busy for t_{PROG} time. PROGRAM EXECUTE command requires 24-bit address with 7 dummy bits and a 17-bit row address.

When CS# goes high, the "PROGRAM LOAD" operation" terminates. Please note the figure below for PROGRAM LOAD.



PROGRAM LOAD (02h) Timing

PROGRAM LOAD x4 (32h): conducts the program with 4 I/O mode



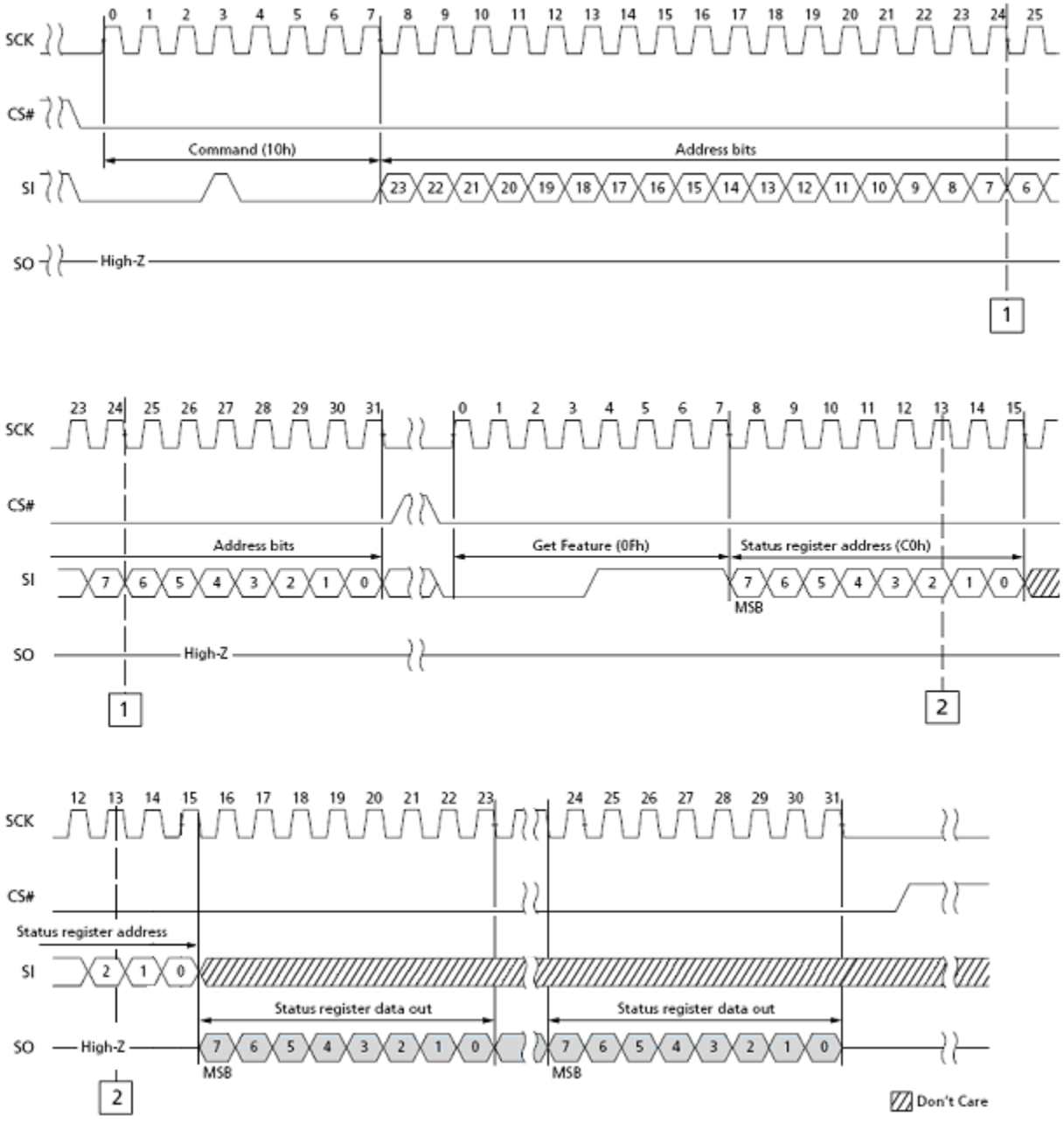
PROGRAM LOAD x4 (32h) Timing

PROGRAM EXECUTE (10h)

After the program data are loaded into the 2,176-Byte Data Buffer (or 2,112 bytes when ECC is enabled), the Program Execute instruction will program the Data Buffer content into the physical memory page that is specified in the instruction. The instruction is initiated by driving the CS# pin low then shifting the instruction code "10h" followed by 7-bit dummy clocks and the 17-bit Page Address into the SI pin. After CS# is driven high to complete the instruction cycle. While the Program Execute cycle is in progress, the Read Status Register (0Fh + C0h) instruction may still be used for checking the status of the OIP bit. The OIP bit is 1 during the Program Execute cycle and becomes 0 when the cycle is finished and the device is ready to accept other instructions again.

Only 4 partial page program times are allowed on every single page.

The pages within the block have to be programmed sequentially from the lower order page address to the higher order page address within the block. Programming pages out of sequence is prohibited.



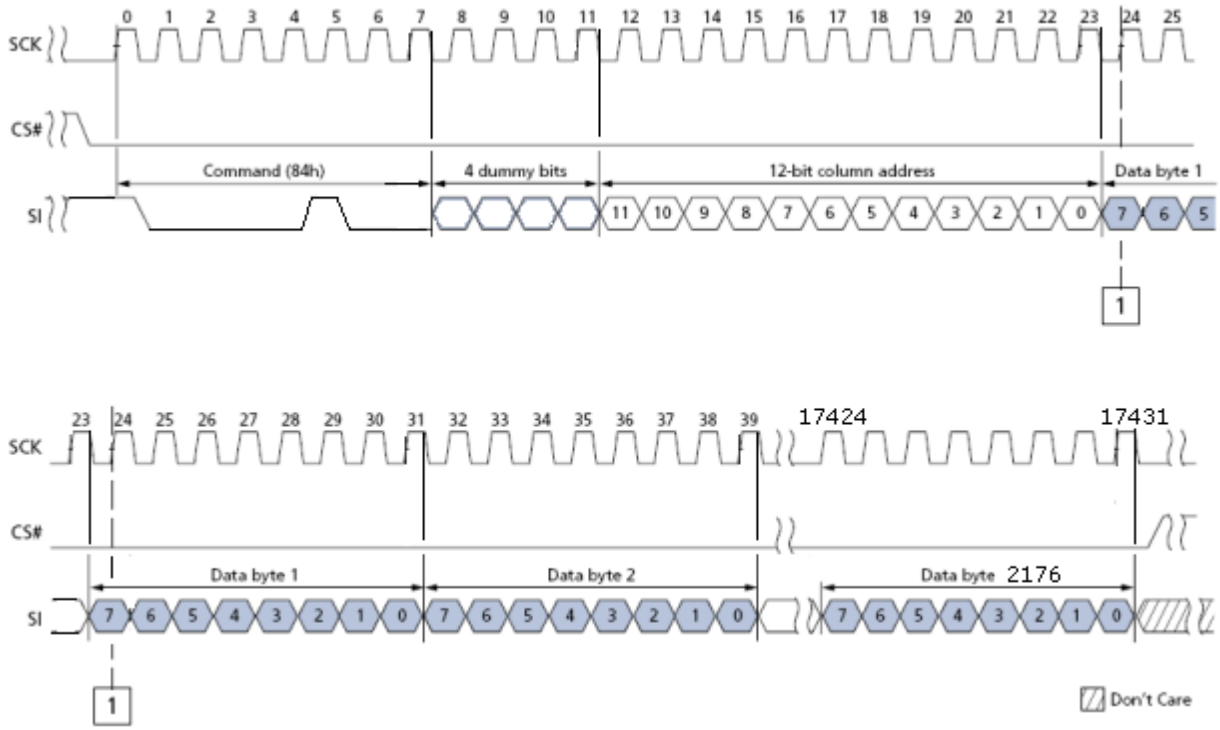
PROGRAM EXECUTE (10h) Timing

PROGRAM LOAD RANDOM DATA x1 (84h)

The command sequence is follows:

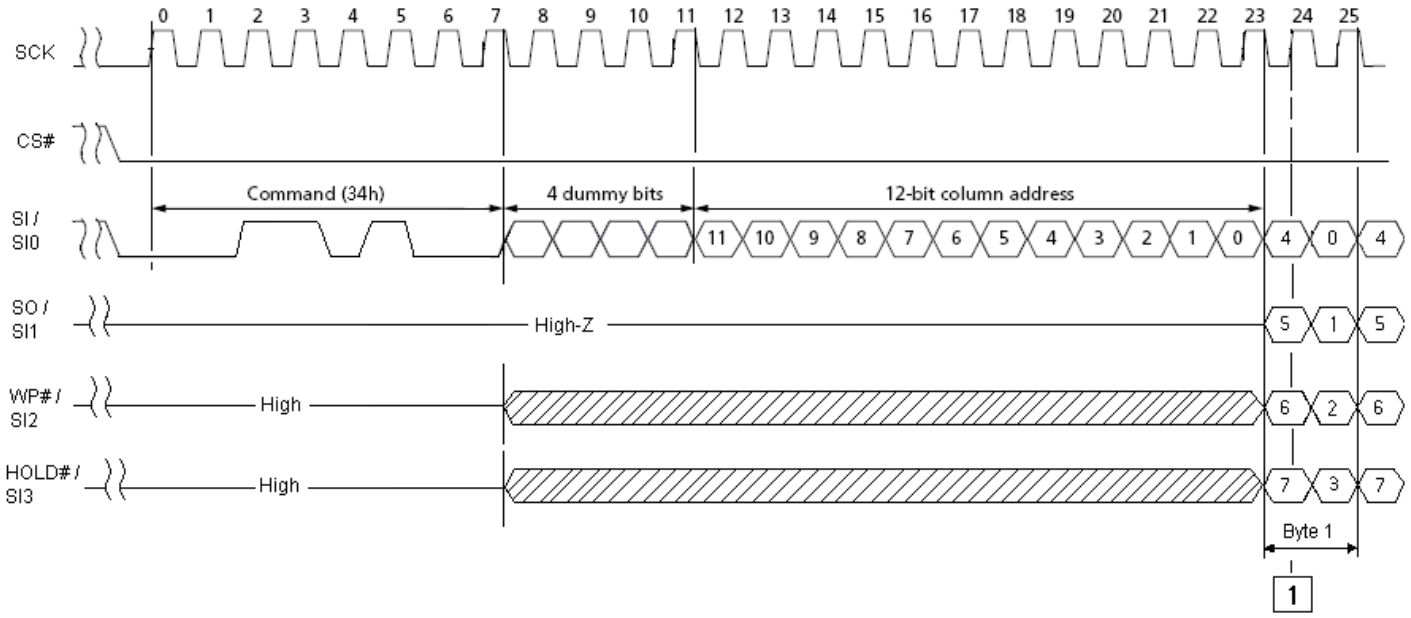
- 06h (WRITE ENABLE)
- 84h (PROGRAM LOAD RANDOM DATA x1) 34h (PROGRAM LOAD RANDOM DATA x4)
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

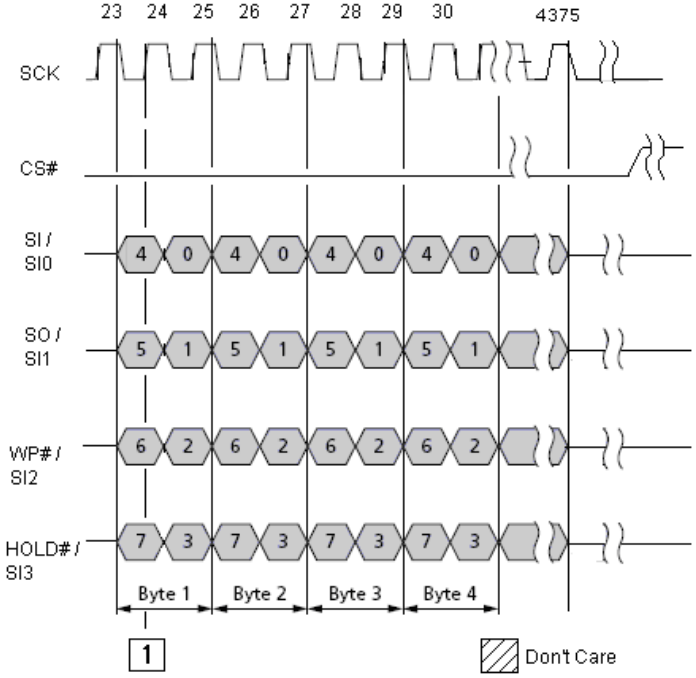
The random data program operation sequence programs or replaces data in a page with existing data. PROGRAM LOAD RANDOM DATA command requires 16-bit address with 4 dummy bits and a 12-bit column address. New data is loaded in the column address provided. If the random data is not sequential, then another PROGRAM LOAD RANDOM DATA command must be issued with a new column address. After the data is loaded, PROGRAM EXECUTE command can be issued to start the programming operation.



PROGRAM LOAD RANDOM DATA (84h) Timing

PROGRAM LOAD RANDOM DATA x4 (34h)





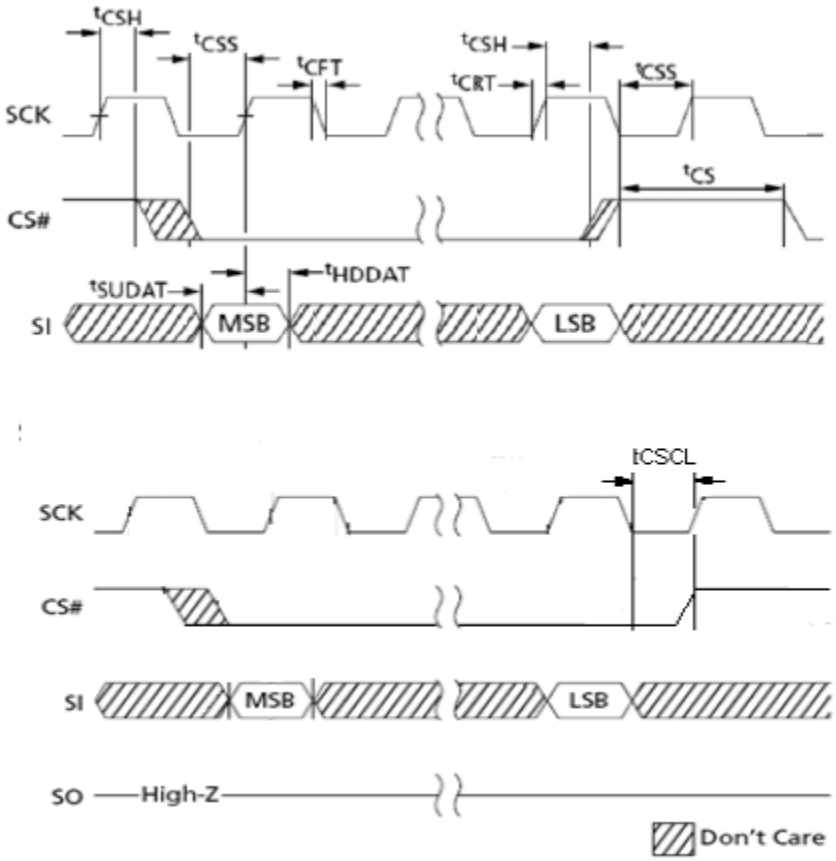
PROGRAM LOAD RANDOM DATA x4 (34h) Timing

Internal Data Move

The command sequence is follows:

- 13h (PAGE READ to cache): to read data from the cell array to internal cache.
- 06h (WRITE ENABLE): to enable the write.
- 84h (PROGRAM LOAD RANDOM DATA x1)
- 34h (PROGRAM LOAD RANDOM DATA x4); to change the data in the internal buffer. This is OPTIONAL in sequence.
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

The INTERNAL DATA MOVE operation sequence programs or rep aces data in a page with existing data. Prior to performing an INTERNAL DATA MOVE operation, the target page content must be read into the cache register. PAGE READ command must be followed with a WRITE ENABLE command to change the contents of memory array.



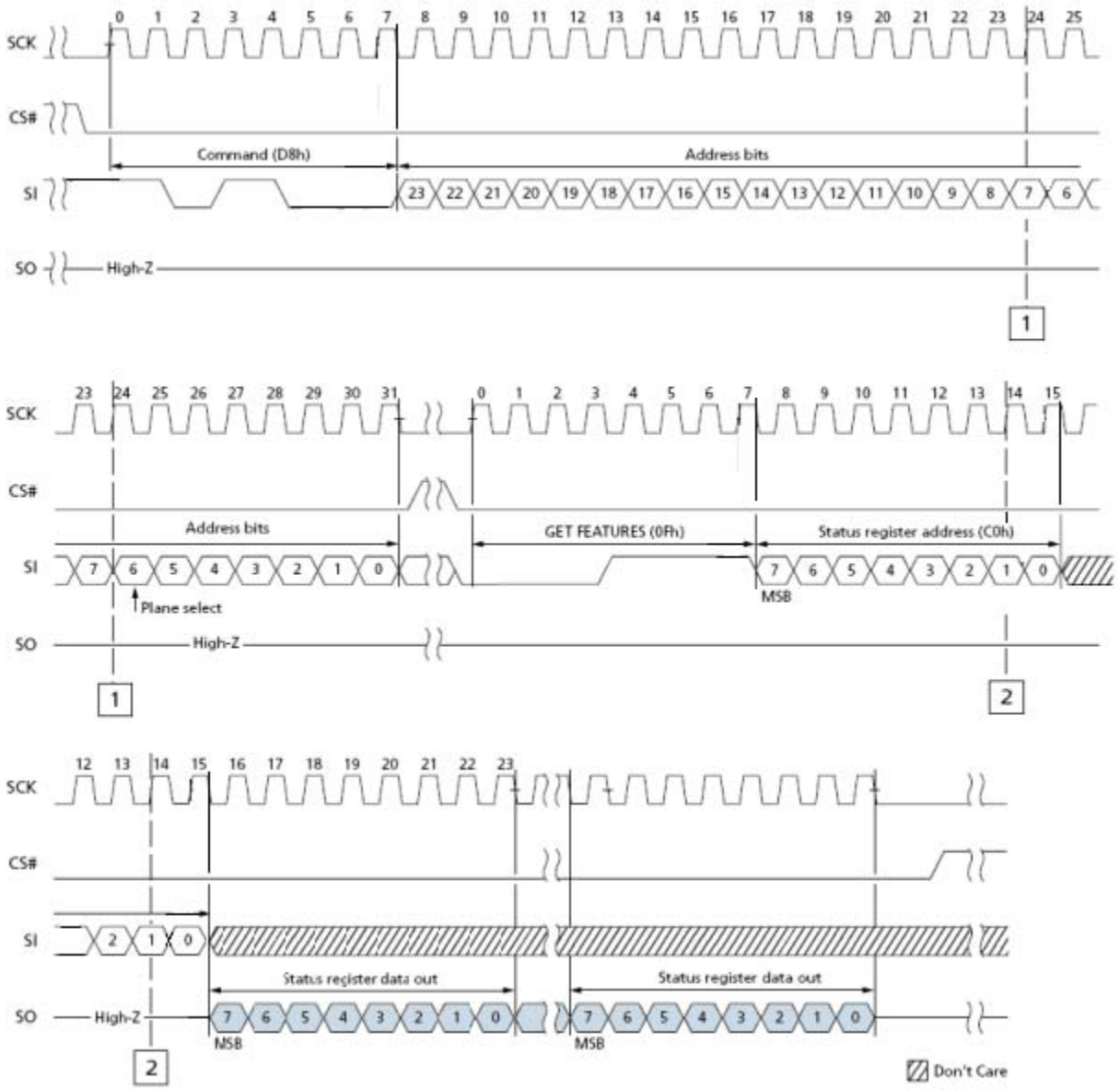
Serial Input and tCSCL Timing

BLOCK ERASE (D8h) Operation

The command sequence is follows:

- 06h (WRITE ENABLE)
- D8h (BLOCK ERASE)
- 0Fh (GET FEATURE command to read the status)

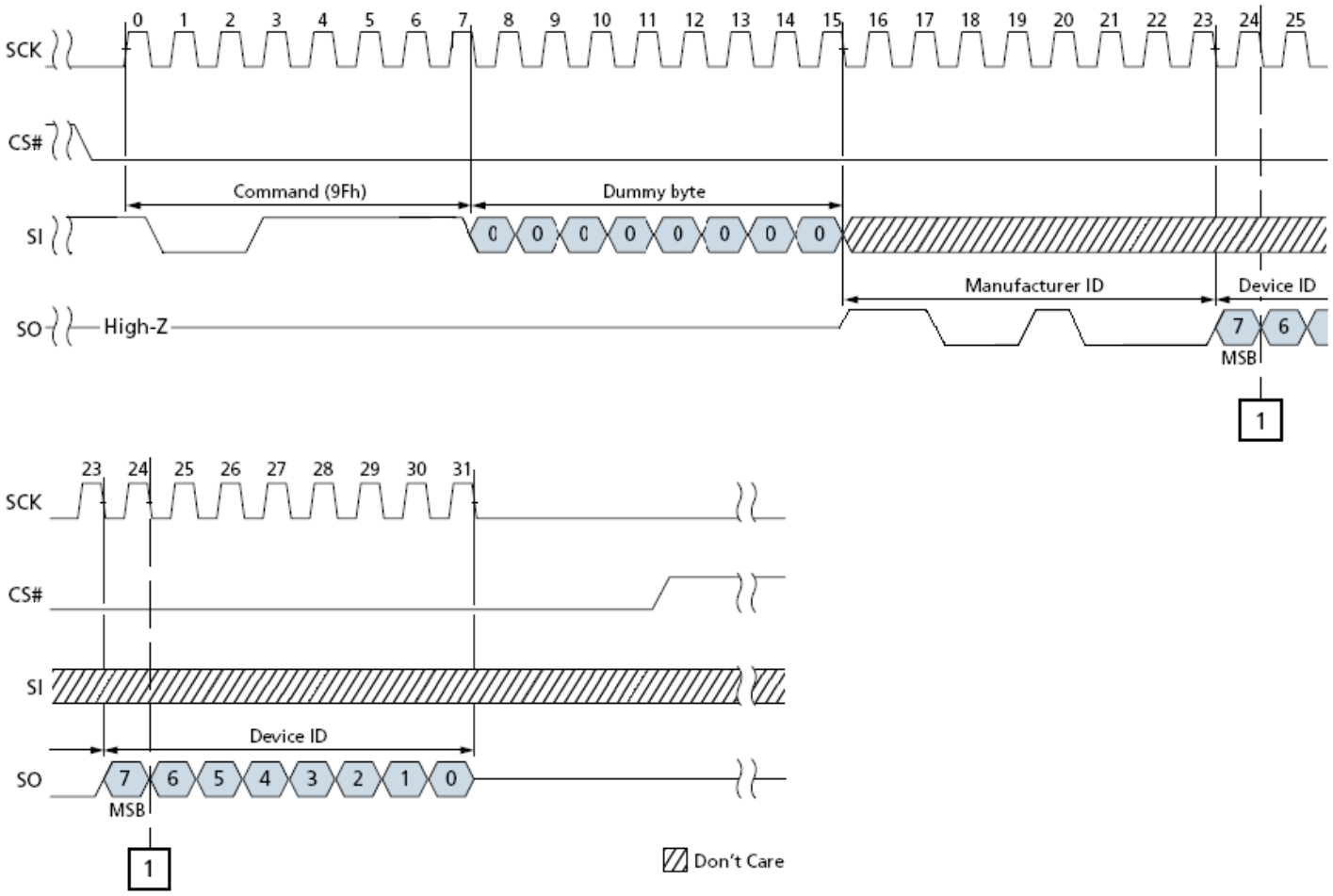
BLOCK ERASE command requires 24-bit address with 7 dummy bits and a 17-bit row address. If WRITE ENABLE command is not issued (WEL bit is not set), then the rest of the erase sequence is ignored. After the row address is registered, the control logic automatically controls the timing and the erase-verify operations, and the device is busy for tBERS time. BLOCK ERASE command operates on one block at a time.



BLOCK ERASE (D8h) Timing

Read ID (9Fh)

The device contains a product identification mode, initiated by writing 9Fh to the command register, followed by an address input of 00h. Five read cycles sequentially output the manufacturer code (C8h), and the device code and 3rd, 4th, 5th cycle ID respectively. The command register remains in Read ID mode until further commands are issued to it.



READ ID Timing

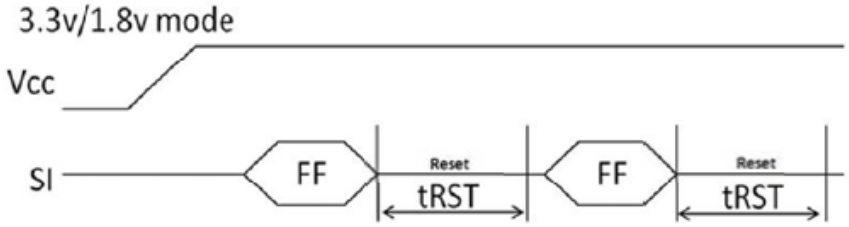
ID Definition Table

Product ID	1st Cycle (Maker Code)	2nd Cycle (Device Code)	3rd Cycle	4th Cycle	5th Cycle
F50D2G41KA (2V)	C8h	51h	7Fh	7Fh	7Fh

	Description
1st Byte	Maker Code
2nd Byte	Device Code
3rd Byte	JEDEC Maker Code Continuation Code, 7Fh
4th Byte	JEDEC Maker Code Continuation Code, 7Fh
5th Byte	JEDEC Maker Code Continuation Code, 7Fh

RESET (FFh)

The RESET (FFh) command stops all operations. For example, in case of a Program or Erase or Read operation, the reset command can make the device enter the wait state.



Reset operation

DPD entry (Deep Power Down, B9h), DPD exit (ABh) and Reload Fuse data

DPD (Deep Power Down) is a low power function that can reduce power consumption by activating DPD mode. It enters from standby only. When the DPD command is executed, the current consumption drops further to Icc2. The command to exit DPD is only accessible during DPD.

Command	Op Code	Address Bytes	Dummy Bytes	Data Bytes
Deep Power Down Entry	B9h	0	0	0
Exit from Deep Power Down	ABh	0	0	0
Reload Fuse data on Standby	ABh	0	0	0

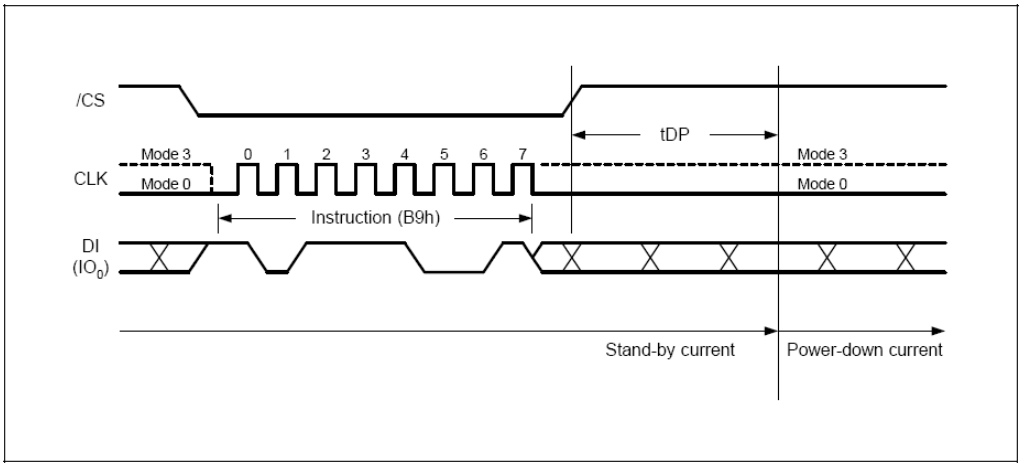
The DPD command is entered during CS# is LOW. CS# must be driven HIGH after the eighth bit of the command code has been latched in. Wait t_{DP} after CS# goes high. Then, the current consumption is reduced to ISB3.

The exit command from DPD is entered during CS# LOW. When CS# goes high, wait t_{RES1} to complete the power on sequence. Then, the device is accessible. Besides, page 0 of block 0 is ready in CACHE.

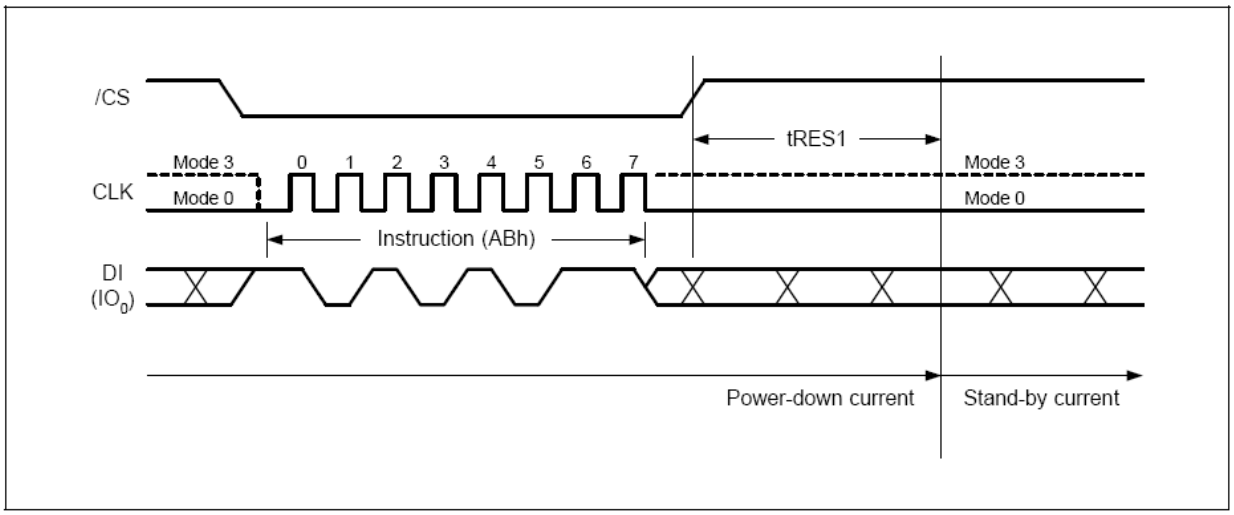
The command that reload Fuse data is entered while CS# is low. After CS# returns high, waits t_{RES1} to complete Fuse load. Then, the device is accessible. Besides, page 0 of block 0 is ready in CACHE.

Note: The B9h & ABh commands are only for single die 2Gb, are not allowed for Dual Die Stacked Operation.

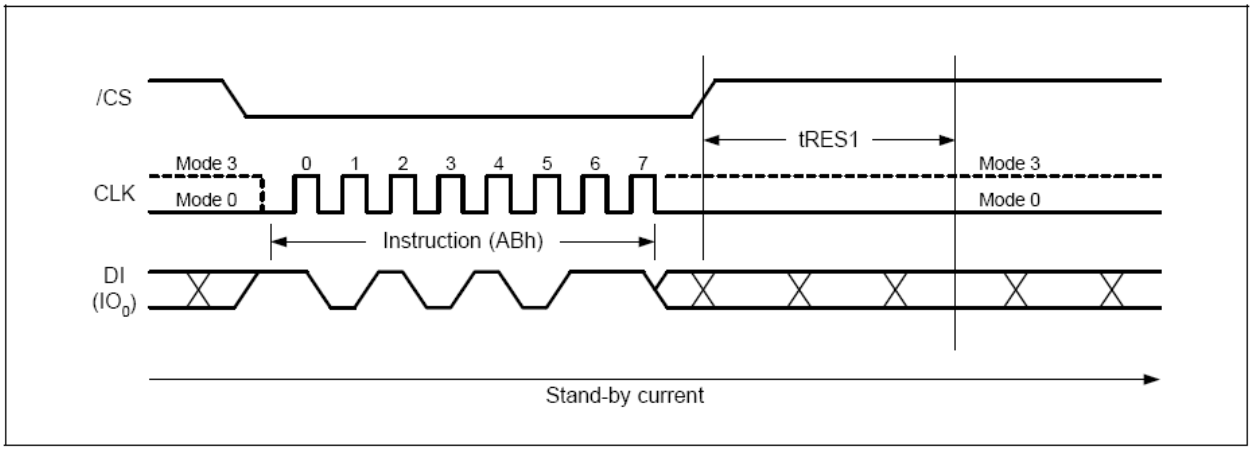
Entry to Deep Power Down

Parameter	Symbol	Max	Unit
CS# High to Power Down Mode	t_{DP}	3	us
	t_{RES1}	1.5	ms

CS# High to Standby Mode without Electronic Signature Read



Exit from Deep Power Down



Reload Fuse data

Boot Read

Boot read is a read to store page 0 of block 0 in CACHE during power on sequence. DATA of page 0 of block 0 is ready in CACHE after the power on cycle.

In case of the exit from DPD, it is automatically ready in CACHE.

Cache Read (31h) and Last Page Cache Read (3Fh)

Cache Read is an extension of Page Read, and is available only within a block. Cache Read will enhance the data throughput by using the Page Buffer. It supports sequential pages to be read out without assigning next page address. After writing the Page Read command (13h) and giving 24-bit address with 7 dummy bits and a 17 bits row address(a row address of Page N is registered), the page data starts the transfer from the main array to the Page Buffer. During this time, GET FEATURE command (C0h, Bit0 OIP Bit) can be issued to monitor the status of the operation.

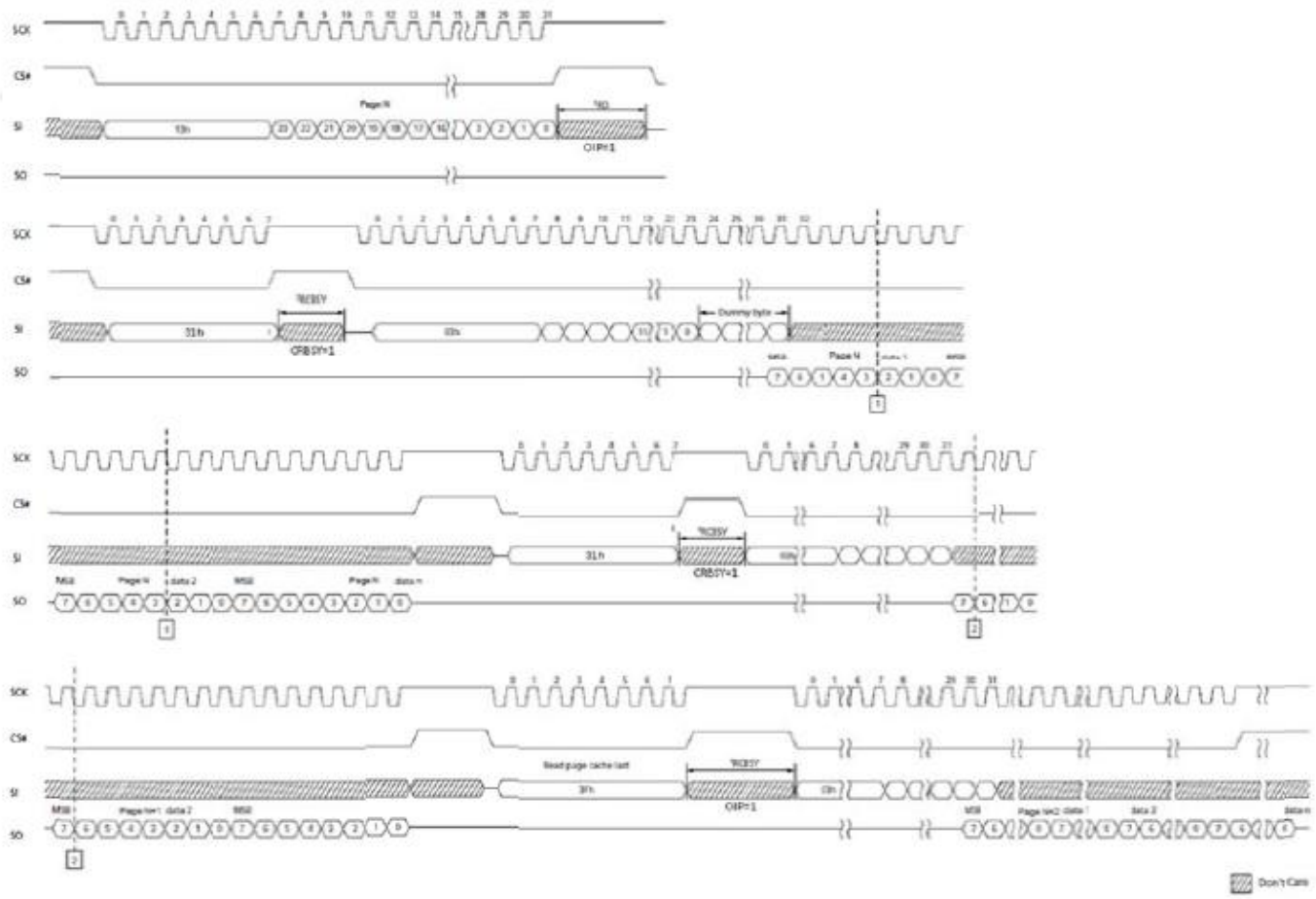
Following a status of successful completion, the Cache Read command (31h) can be issued, data of the designated page (Page N) are transferred from Page Buffer to Cache Register . During this time, GET FEATURE command (C0h, Bit0 OIP Bit) can be issued to monitor the status of the operation and to indicate if the Cache Register is available.

Then following the Read from Cache command (03h/0Bh/3Bh/6Bh/BBh or EBh) may get the designated page (Page N) data output from Cache Register. At the same time, the Next Page (Page N+1) are transferred from array to Page Buffer.

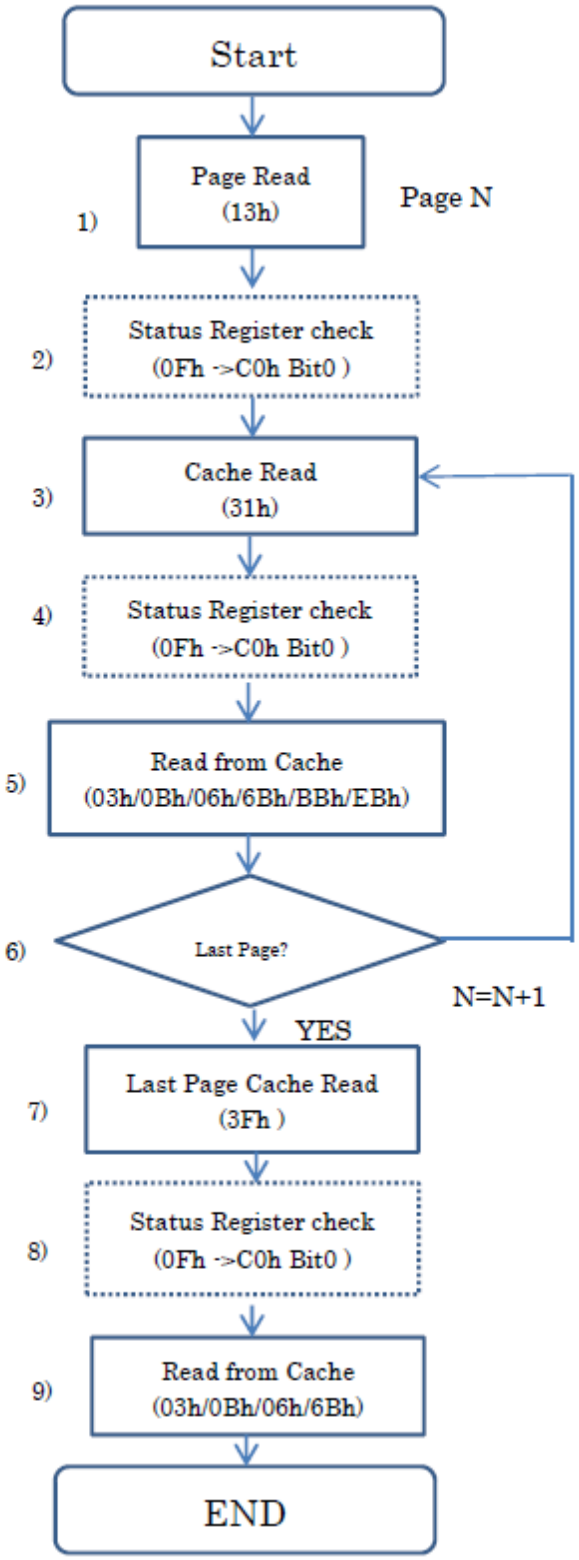
To confirm the last page to be read-out during the Cache Read, the Last Page Cache Read command (3Fh) is used to stop the data transfer from array to Page Buffer.

The command sequence is follows:

1. Page read(13h)_PageN (+ 7 dummy bits + 17bits row address)
2. GetFeatureC0(OIP=0)
3. Cache Read (31h)_PageN+1
4. GetFeatureC0(OIP=0)
5. Read from CACHE 03h/0Bh/3Bh/6Bh/BBh/EBh _PageN (+4 dummy bits + 12 bits column address+ dummy bytes)
6. Repeat 3)->5) for previous Page data Until last page
7. Last Page Cache Read (3Fh) _Page Last (+ 7 dummy bits + 17bits row address)
8. GetFeatureC0(OIP=0)
9. Read 03h/0Bh/3Bh/6Bh/BBh/EBh _last Page
   (+4 dummy bits + 12bits row address+ dummy bytes)


SCK
CS#
SI
SO
Page N
tRD
OIP=1
tWCBSY
31h
Dummy byte
CRBSY=1
Page N
tWCBSY
31h
CRBSY=1
Read page cache last
tWCBSY
31h
OIP=1
Don't Care

Cache Read



Cache Read (31h) Flow

Cache Read Random Page (30h)

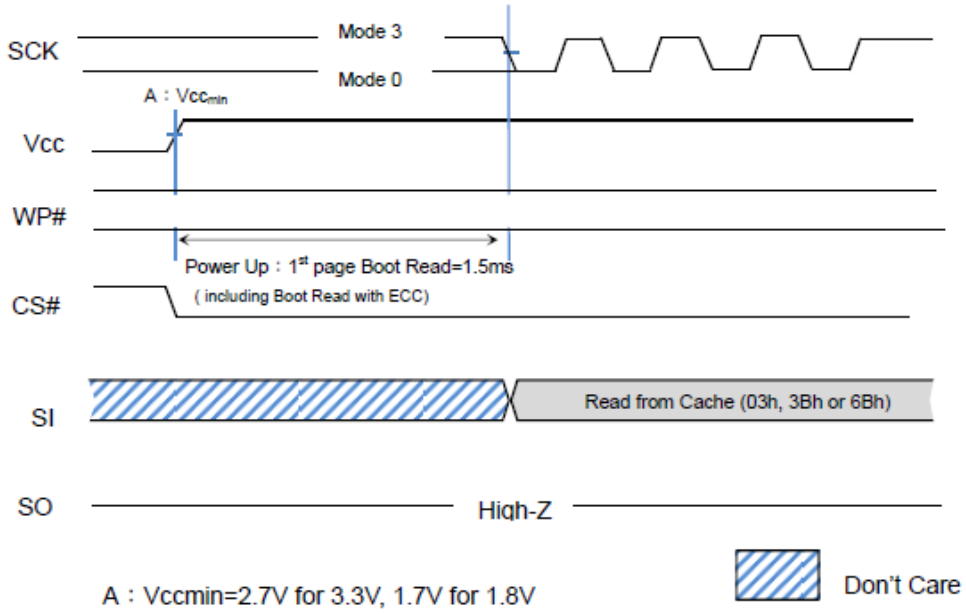
Cache Read command reads the pages of the same block sequentially without assigning next Page's address. On the other hand, Cache Read Random Page can assign the specified page of the same block to be read out. The specified pages to be read out next by assigning a 24-bit address with 7 dummy bits and a 17 bits row address.

The command sequence is follows:

1. Page read(13h)_PageX (+ 7 dummy bits + 17bits row address)
2. GetFeatureC0(OIP=0)
3. Cache Read Random Page(30h)_PageY (+ 7 dummy bits + 17bits row address)
4. GetFeatureC0(OIP=0)
5. Read from CACHE 03h/0Bh/3Bh/6Bh/BBh/EBh _PageX (+4 dummy bits + 12 bits column address+ dummy bytes)
6. Repeat 3)->5) for previous Page data Until last page
7. Last Page Cache Read(3Fh) _Page Last (+ 7 dummy bits + 17bits row address)
8. GetFeatureC0(OIP=0)
9. Read 03h/0Bh/3Bh/6Bh/BBh/EBh _last Page
   (+4 dummy bits + 12 bits column address+ dummy bytes)

Power Up Timing

During power transitions, V_{CC} is internally monitored. After V_{CC} has reached V_{CC}min, the device automatically performs the RESET command. The first access can occur 1.5ms after V_{CC} reaches V_{CC}min, and the required command can be issued to the device.



Power Up and Reset Timing

ECC Protection

ECC is enabled after device power-up, so the default PROGRAM and READ commands operate with internal ECC in the active state.

During a PROGRAM operation, the device calculates an ECC code on the 2KB page in the cache register, before the page is written to the NAND Flash array. The ECC code is stored in the spare area of the page in array.

During a READ operation, the page data is read from the array to the cache register, where the ECC code is calculated and compared with the ECC code value read from the array. If a single-bit data error is discovered, the error is corrected in the cache register and only the corrected data is on the output bus.

Spare 0~3 are for user data 0~3 and internal ECC is stored in Spare Area (840h~87Fh). When the internal ECC is disabled, all are for user data.

Max Bytes Column Address	Min Bytes Column Address	ECC protected	Area	Description
1FFh	000h	Yes	Main 0	User data 0 (512 bytes)
3FFh	200h	Yes	Main 1	User data 1 (512 bytes)
5FFh	400h	Yes	Main 2	User data 2 (512 bytes)
7FFh	600h	Yes	Main 3	User data 3 (512 bytes)
80Fh	800h	Yes	Spare 0	User meta data 0 2) (16 bytes)
81Fh	810h	Yes	Spare 1	User meta data 1 (16 bytes)
82Fh	820h	Yes	Spare 2	User meta data 2 (16 bytes)
83Fh	830h	Yes	Spare 3	User meta data 3 (16 bytes)
87Fh (2175)	840h (2112)	Yes	Spare Area 1	Internal ECC parity data (64 bytes)

Note:

1. Only for internal ECC if internal ECC is enabled. The ECC parity code generated by internal ECC is stored in column addresses 2112-2175 and the users cannot access to these specific addresses when internal ECC is enabled.
2. Some bytes for bad block marker. While using the Partial Page Program, the users must program the data to main area and spare area simultaneously by the definition of data pair.

Error Management

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed. The information regarding the initial invalid blocks is called the initial invalid block information. Devices with initial invalid blocks have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block does not affect the performance of valid blocks because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid blocks via address mapping.

The 1st block, which is placed on 00h block address, is guaranteed to be a valid block up to 1K program/erase cycles with 8bits/512Byte ECC.

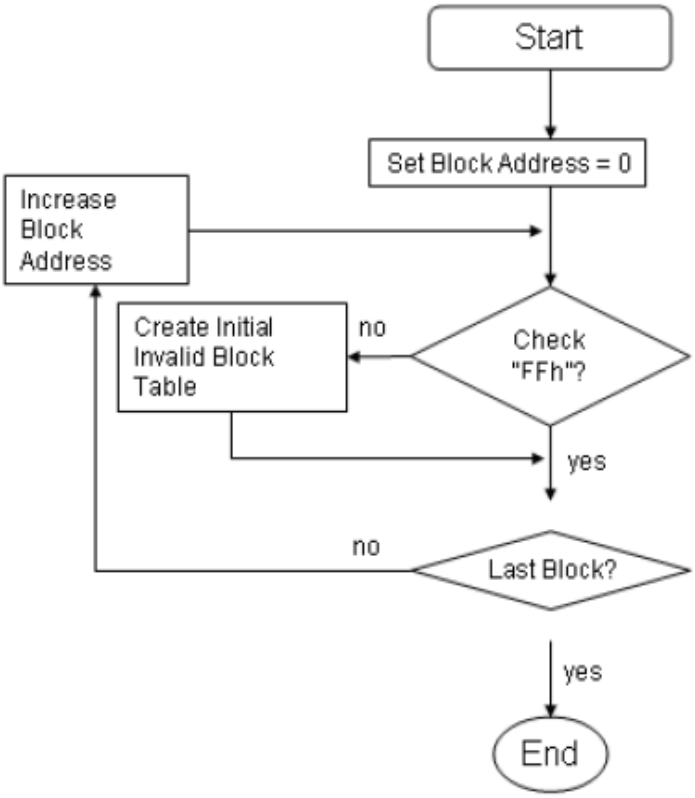
Unpredictable behavior may result from programming or erasing the defective blocks. Figure illustrates an algorithm for searching factory-mapped defects, and the algorithm needs to be executed prior to any erase or program operations.

A host controller has to scan blocks from block 0 to the last block using page read command and check the data at the column address 2048 of page 0 and page 1. If the read data is not FFh, the block is interpreted as an invalid block. Do not erase or program factory-marked bad blocks. The host controller must be able to recognize the initial invalid block information and to create a corresponding table to manage block replacement upon erase or program error when additional invalid blocks develop with Flash memory usage.

Description	Requirement
Minimum / Maximum number of valid block number of block	2008 / 2048
Bad block mark	Non FFh
Mark location	Column 2048 of page 0 and page 1

Note:

1. The device may include initial invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits which cause status failure during program and erase operation. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of initial invalid blocks.
2. Read FFh check is at the 1st byte of the 1st and 2nd pages of the block spare area.
3. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment and is guaranteed to be a valid block up to 1K program/erase cycles with 8bits/512Byte ECC.



Check “FFh” at column address 2048 of the first page and the second page

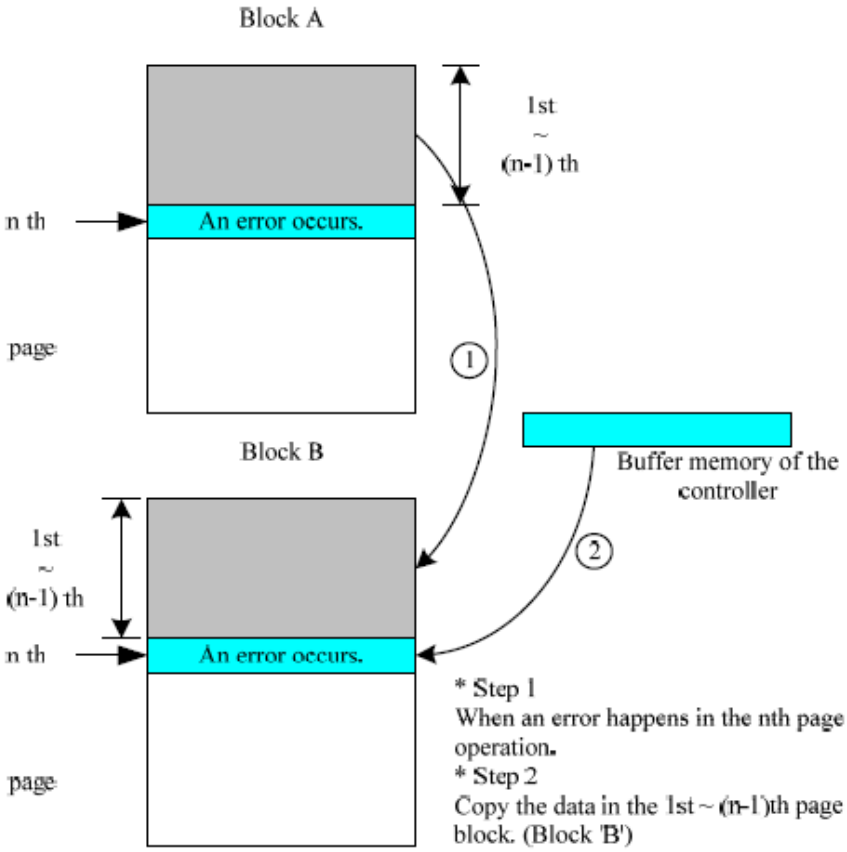
```
For (i=0; i<Num_of_LUs; i++)
{
      For (j=0; j<Blocks_Per_LU; j++)
      {
            Defect_Block_Found=False;

            Read_Page(lu=i, block=j, page=0);
            If (Data[coloumn=First_Byte_of_Spare_Area]!=FFh) Defect_Block_Found=True;

            Read_Page(lu=i, block=j, page=1);
            If (Data[coloumn=First_Byte_of_Spare_Area]!=FFh) Defect_Block_Found=True;

            If (Defect_Block_Found) Mark_Block_as_Defective(lu=i, block=j);
      }

  }
```

Algorithm for Bad Block Scanning

Block Replacement

Within its lifetime, number of invalid blocks may increase with NAND Flash memory. Refer to the qualification report for the actual data. The following possible failure modes should be considered to implement a highly reliable system. In the case of failure after ERASE or PROGRAM in Status Register (Erase_Fail or Program_Fail), Block Replacement should be done. Because PROGRAM status fail during a Page Program does not affect the data of the other Pages in the same block, Block Replacement can be executed with a Page-sized buffer by finding an erased empty Block and reprogramming the current target data and copying the rest of the replaced block.

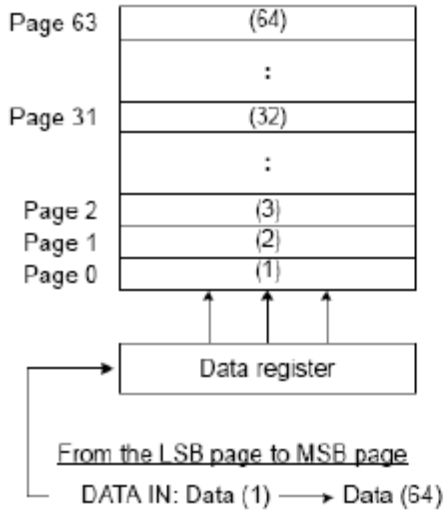
In case of READ, ECC must be employed. To improve the efficiency of memory space, it is recommended that the Read or verification failure due to Single Bit error be reclaimed by ECC without any block replacement.

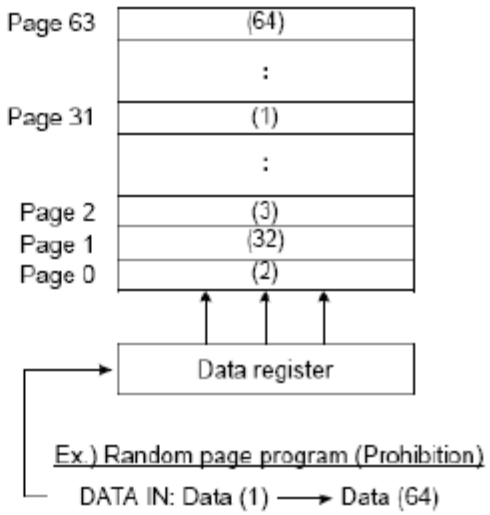


* Step 1
When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step 2
Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
* Step 3
Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'
* Step 4
Do not erase or program to Block 'A' by creating an 'invalid block' table or other appropriate scheme.

Addressing for Program Operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) pages of the block. Random page address programming is prohibited. In this case, the definition of LSB page is the LSB among the pages to be programmed. Therefore, LSB page doesn't need to be page 0.





Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{CC}	-0.6 to +2.45	V
	V_{IN}	-0.6 to +2.45	
	$V_{I/O}$	-0.6 to Vcc+0.3(<2.45V)	
Temperature Under Bias	T_{BIAS}	-40 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Short Circuit Current	I_{OS}	5	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

(Voltage reference to GND, T_A = -40 to +105°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	1.7	1.8	1.95	V
Supply Voltage	V_{SS}	0	0	0	V

DC and Operation Conditions

(Recommended operating conditions otherwise noted)

Parameter		Symbol	Test Conditions	Min.	Typ.[2]	Max.	Unit
Operating Current	Page Read with Serial Access	I_{CC1}	CS#=V_{IL}, I_{OUT}=0mA	-	26	30	mA
	Program	I_{CC2}	-	-	20	25	
	Erase	I_{CC3}	-	-	20	25	
Stand-by Current (TTL)		I_{SB1}	CS#=V_{IH}, WP#=0V/V_{CC}	-	-	1	mA
Stand-by Current (CMOS)		I_{SB2}	CS#= V_{CC} -0.2, WP#=0V/ V_{CC}	-	10	50	uA
Power Down Current		I_{SB3}	CS#=V_{CC}-0.2, WP#=0V/V_{CC}, SCK=0V/V_{CC}	-	1	5	
Input Leakage Current		I_{LI}	V_{IN}=0 to V_{CC} (max)	-	-	±10	uA
Output Leakage Current		I_{LO}	V_{OUT}=0 to V_{CC} (max)	-	-	±10	uA
Input High Voltage		V_{IH}[1]	-	0.8 x V_{CC}	-	V_{CC} +0.3	V
Input Low Voltage, All inputs		V_{IL}[1]	-	-0.3	-	0.2 x V_{CC}	V
Output High Voltage Level		V_{OH}	I_{OH}= -100uA	V_{CC} -0.1	-	-	V
Output Low Voltage Level		V_{OL}	I_{OL}=+100uA	-	-	0.1	V

Note:

1. V_{IL} can undershoot to -0.4V and V_{IH} can overshoot to V_{CC}+0.4V for durations of 20ns or less.
2. Typical value are measured at V_{CC} = 1.8V, T_A=25℃. Not 100% tested.

AC Test Condition

(T_A=-40 to +105°C, V_{CC}= 1.7V~1.95V)

Parameter	Condition
Input Pulse Levels	0 to V_{CC}
Input Rise and Fall Times	Max: 2.4ns
Input and Output Timing Levels	V_{CC} /2
Output Load	1 TTL Gate and C_L=15pF

Capacitance

(T_A=25°C, V_{CC}= 1.8V, f=1.0MHz)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input / Output Capacitance	$C_{I/O}$	V_{IL} = 0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	-	8	pF

Note: Capacitance is periodically sampled and not 100% tested.

Read / Program / Erase Timing Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Average Program Time	t_{PROG}	-	400	900	us
Number of Partial Program Cycles in the Same Page	NOP	-	-	4	Cycle
Block Erase Time	t_{BERS}	-	4	10	ms
Data Transfer from Cell to Register with Internal ECC	t_{RD}	-	-	130	us
Data Transfer from Cell to Register without Internal ECC	t_{RD1}	-	-	25	us

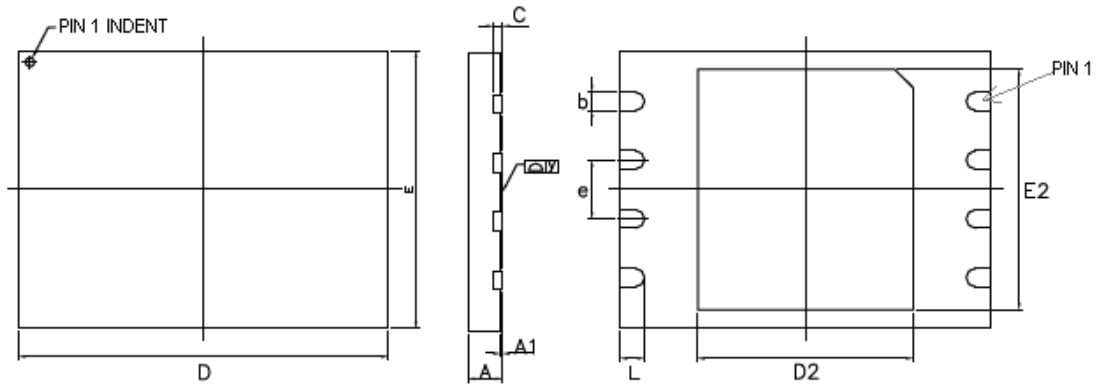
General Timing Characteristic

Parameter		Symbol	Min.	Max.	Unit
Clock frequency	104MHz	f_C		104	MHz
	83MHz	f_C		83	MHz
Hold# non-active hold time relative to SCK		t_{CD}	4.5		ns
Hold# hold time relative to SCK		t_{CH}	4.5		ns
Command deselect time		t_{CS}	80		ns
CS# Setup Time		t_{CSS}	6		ns
CS# Hold Time		t_{CSH}	4		ns
The last valid Clock low to CS# high		t_{CSCL}	5		ns
Output disable time		t_{DIS}		20	ns
Hold# non-active setup time relative to SCK		t_{HC}	4.5		ns
Hold# setup time relative to SCK		t_{HD}	4.5		ns
Data input setup time		t_{SUDAT}	2		ns
Data input hold time		t_{HDDAT}	3		ns
Output hold time		t_{HO}	2		ns
Hold# to output Hi-Z		t_{HZ}		9	ns
Hold# to output Low-Z		t_{LZ}		9	ns
Clock low to output valid	104MHz	t_V		9	ns
	83MHz	t_V		12	ns
Clock high time		t_{WH}	4		ns
Clock low time		t_{WL}	4		ns
Clock rise time (slew rate)		t_{CRT}	0.1		V/ns
Clock fall time (slew rate)		t_{CFT}	0.1		V/ns
WP# setup time		t_{WPS}	20		ns
WP# hold time		t_{WPH}	100		ns
Resetting time during Idle/Read/Program/Erase		t_{RST}		5/5/10/500	us

Note: Fast Read x2 IO (BBh) & (BCh) and Fast Read x4 IO (EBh) & (ECh) can run up to 40MHz at 1.8V.

PACKING DIMENSIONS

8-Contact WSON (8x6 mm)

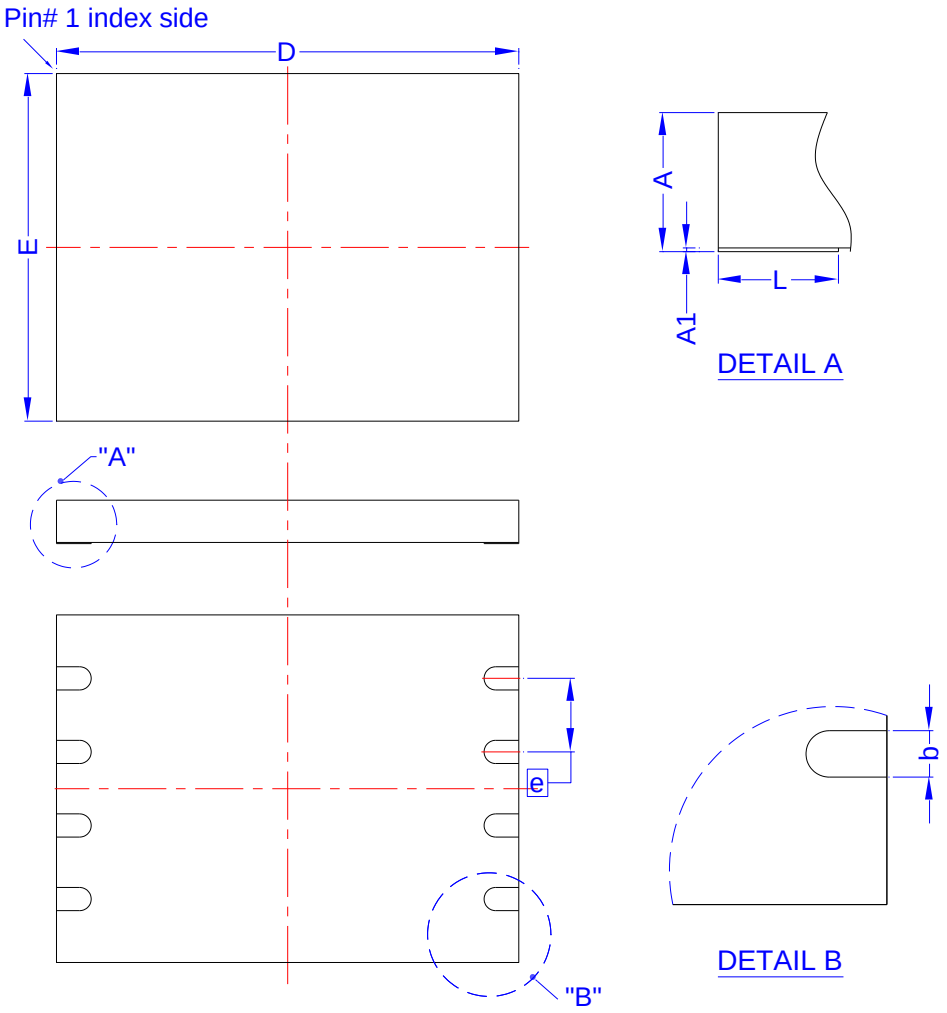


SYMBOL	MILLIMETERS			INCHES		
	Min	Normal	Max	Min	Normal	Max
A	0.70	0.75	0.8	0.028	0.03	0.031
A1	0.00	0.035	0.05	0.000	0.001	0.002
b	0.35	0.40	0.45	0.014	0.016	0.018
C	0.19	0.20	0.25	0.007	0.008	0.010
D	7.90	8.0	8.10	0.311	0.315	0.319
D2	3.35	3.40	3.45	0.132	0.134	0.136
E	5.90	6.0	6.10	0.232	0.236	0.240
E2	4.25	4.30	4.35	0.167	0.168	0.171
e	1.27BSC			0.05BSC		
L	0.40	0.50	0.60	0.016	0.020	0.024
y	0.00	…	0.08	0.000	…	0.003

NOTE: BSC, Basic lead spacing between centers.

PACKING DIMENSIONS

8-Contact WSON (8x6 mm) without expose metal pad



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.35	0.40	0.45	0.014	0.016	0.018
D	7.90	8.00	8.10	0.311	0.315	0.319
E	5.90	6.00	6.10	0.232	0.236	0.240
e	1.27 BSC			0.050 BSC		
L	0.40	0.50	0.60	0.016	0.020	0.024

Controlling dimension: millimeter
(Revision date: Apr 25 2018)

Revision History

Revision	Date	Description
1.0	2025.12.23	Original

Important Notice

The contents contained in this document are believed to be accurate at the time of publication. ESMT assumes no responsibility for any error in this document, and reserves the right to change the products or specification in this document without notice.

The information contained herein is presented only as a guide or examples for the application of our products. No responsibility is assumed by ESMT for any infringement of patents, copyrights, or other intellectual property rights of third parties which may result from its use. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of ESMT or others.

Any semiconductor devices may have inherently a certain rate of failure. To minimize risks associated with customer's application, adequate design and operating safeguards against injury, damage, or loss from such failure, should be provided by the customer when making application designs.

ESMT's products are not authorized for use in critical applications such as, but not limited to, life support devices or system, where failure or abnormal operation may directly affect human lives or cause physical injury or property damage. If products described here are to be used for such kinds of application, purchaser must do its own quality assurance testing appropriate to such applications.